Ambient Light Effect on Receiver for Visible Light Communication Systems

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Highlights
• This paper focuses on artificial light effect for VLC systems.
• A theoretical framework is given to observe problem condition in the study.
• A practical solution was proposed to overcome the problem by caused artificial light effect.

Article Info

Abstract

The visible light communication (VLC), which can simultaneously provide both the lighting and the data transmission at the same time, has been emerged as a wireless optical communication technology. This article investigates the performance of VLC systems under ambient light effect that can cause receiver saturation. When reach to saturation the receiver, data bits cannot be correctly detected at the receiver side. This is because ambient light will decrease the difference between logical '1' and '0' levels when occur the saturation caused by ambient light. This paper offers a framework to demonstrate the ambient light effect for VLC systems. In addition to this, ambient light effect is observed for both hard decision and soft decision receiver schemes in the simulation results. It is shown from simulation results that BER performance decreases when the ambient light level increase and saturate the receiver. Moreover, an experimental system is set up to observe the problem status. A hybrid structure, which consists of Field Programmable Gate Arrays (FPGA) and analog circuits, is implemented on receiver side to amplify the photodiode current and to decrease the ambient light effect.

1. INTRODUCTION

As a consequence of increasing wireless-based systems and internet-sharing devices, communication technologies need an abundant spectrum to cope with the continuous availability of high data traffic. In particularly, the massive growth in the wireless data sharing has inspired to appear the alternative communication systems to Radio Frequency (RF). In this sense, the visible light communication (VLC) technology that is one of the optical communication systems has received the much attention from many researchers to meet the exploding demand for both spectral band and high speed data sharing. Therefore, it is considered that the VLC is a significant candidate for future wireless optical systems since it can support the multiplexing techniques such as orthogonal frequency-division multiplexing (OFDM), code division multiple access (CDMA), time-division multiple access TDMA [1-3].

Various alternative ways have been proposed for driving the LEDs in VLC systems [4, 5]. On-Off Keying (OOK) method is one of the most basic modulation techniques for Optical Wireless Communication (OWC) systems to apply to driving circuits of LEDs since it generates the logical level signal dependent on the data bits being 1 or 0. However, the OOK technique requires detection threshold or logic level classification techniques to provide the user mobility for estimating of information bits [6]. This is one of the most important disadvantages of OOK scheme. In addition to this, it is observed from references [7-12] that BER performance of OOK suffer from the ambient light effect since ambient light causes a fluctuation at the threshold level. Hence, various modulation schemes have been improved to detect data bits without using any threshold value. One of these modulation techniques is pulse position modulation (PPM) method [13]. By using Pulse Width Modulation (PWM) method, OOK and PPM techniques have been modified to adjust

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the dimming level of LED. The modified OOK and PPM schemes are referred to as Variable OOK (VOOK) and Variable PPM (VPPM) [5].

It is expected that VLC systems provide high transmission rate and support the bandwidth efficiency to meet the huge data sharing for next generation communication technologies. The experimental VLC systems have been widely investigated to implement on the present indoor communication systems. In particular, high-speed circuits are the promising systems to supply the end user requirements related to high speed data sharing [14]. It is greatly explored the FPGA-based VLC transceiver systems to ensure high speed data transmission. In this sense, a multiuser system that performs CDMA technology has been improved to provide 625 Mb/s data rate [15]. In another paper that is used OFDM system, authors have been achieved data rate of 1.84Gbit/s for the future heterogeneous in-house network [16]. The authors of [17] have been further developed the data rate of VLC links to implement on underwater communication systems. The data rate of improved FPGA-based system that has BER performance of 3.5×10^{-3} reaches to 2.34Gbit/s over transmission distance of 2.5m. In [18], FPGA-based 32-QAM (Quadrate Amplitude Modulation) scheme have been implemented on the experimental OFDM-VLC system to provide data rate of 3.63-Gb/s with BER at below 3.8×10^{-3}.

One of the important disadvantages of visible light communication systems, which has gained importance in recent years, is the DC interferences caused by ambient lights such as daylight, LED lamps and mobile phone screen lighting [19]. In the literature various methods have been proposed to eliminate the effect of this interference caused by ambient lights. The one of these methods is to filter the DC component by putting a capacitor in input of receiver. However, this method causes a delay in the transmission for data signal [8]. In another method, it is used a differential amplifier and subtracted a positive DC voltage from the voltage signal that is obtained at the output of the transimpedance amplifier [9]. In a similar way, it can be summed a negative DC voltage with the output signal of the transimpedance amplifier [10]. In addition to these methods, high-pass filters can be employed to eliminate the interference caused by ambient lights of which frequency is very low [11]. To decrease the effect of DC ambient light, besides, it is also included the applying active feedback between input and output and the using active inductors in the literature [12].

In the literature, it is considered that ambient light is defined as D.C. level signal under non-mobile conditions [7, 12]. Hence, the BER performance of PPM cannot affect from variable D.C. level since the DC level is equally added to all PPM slots [20]. However, it can be claimed that the performance of PPM scheme can decrease for practical systems when semiconductor devices reach to saturation level at the receiver side [4]. This is because it will be decreased the difference between filled slot level and empty slot level. The automatic gain controller schemes were proposed to alleviate this problem [21, 22]. The authors in reference [21] adjusted the external reference voltage to control the gain of receiver circuit while authors of paper [22] used a variable resistor to adjust the amplitude of output signal. However, mobility condition cannot be provided by user-controlled adjustable systems. Hence, this paper focuses on how the saturation effect can be decreased to provide data transmission under ambient light effect. The main contributions of this paper are summarized as follows:

- In our paper, we investigated the ambient light effect on VLC-receivers under saturation condition. Under ambient light condition, it is considered that empty slot level can rise while filled slot level can approach to saturation level of amplifier. The difference between empty and filled slots can decrease at the output of amplifier. This effect will decrease the transmission performances of many modulation schemes, including OOK and PPM.
- For the first time, it is investigated the DC ambient light effect on PPM transmission scheme under receiver-saturation condition. In addition to this, it has been performed a theoretical framework for receiver-saturation in 2-PPM transceiver systems.
- To indicate the effect of ambient light on PPM systems, the transceiver system is implemented on Xilinx FPGA board. A hybrid transceiver, which is including both analog and digital systems, is integrated on VLC technology in the paper.

2. PROBLEM STATEMENT

The theoretical studies can present the ambient light as Direct-Current (DC) [7, 12]. However, the condition can be invalid for practical applications. Therefore, an amplifier and converter circuit must be used to increase the photodiode current and convert it to voltage in VLC systems. The amplitude level of logical '1' cannot be affected from ambient light since the saturation condition is available due to amplifier. However, the amplitude level of logical '0' can rise to saturation level when the optical power of ambient light is increased. The problem can be observed for many modulation methods because the ambient light can increase only amplitude level of logical '0'.
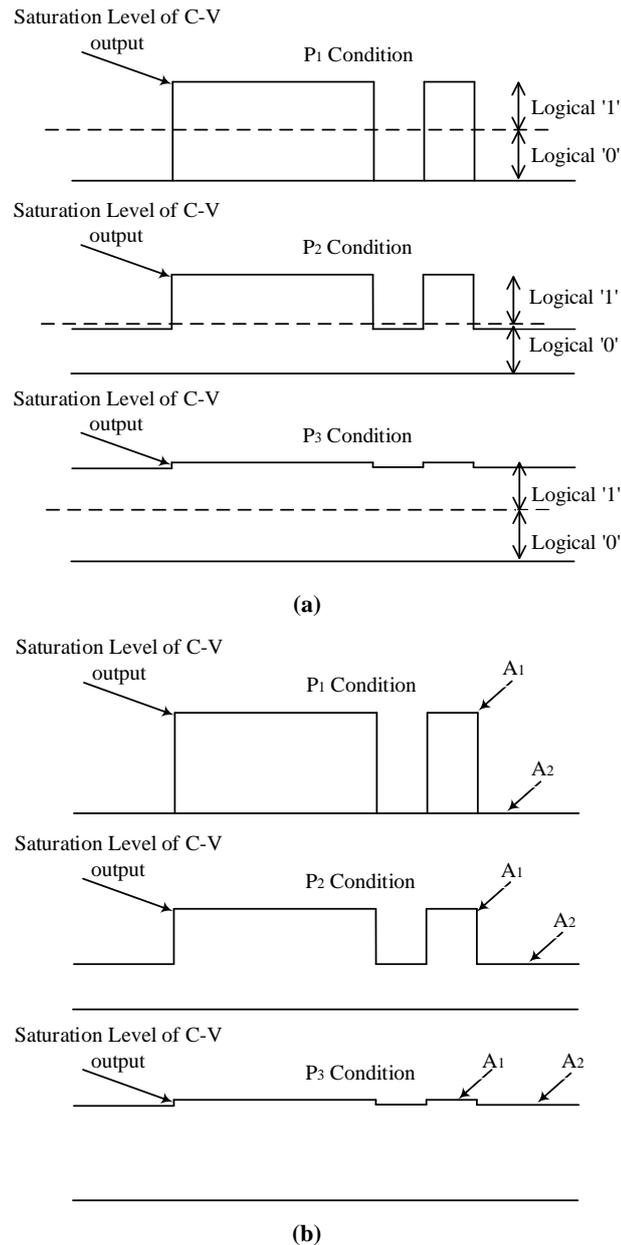

Figure 1. *The comparison of logical '1' and logical '0' under variable ambient light power. (a) logical level demodulator (hard decision), (b) Integral based demodulator (Soft Decision)*

For example, the traditional PPM technique consists of single filled slot. The ambient light fills the empty slot to saturation level while filled slots is keeping steady at saturation level. Therefore, the detection of filled slot can be difficult. Figure 1 is given to define the problem Situation.

In Figure 1, the P_1, P_2, and P_3 are defined as optical power of ambient light. The C-V Converter is defined as Current-Voltage Converter. The orders of optical ambient light powers are follows: $P_3>P_2>P_1$. As shown in the Figure 1.a, logical '0' level is approach to saturation level or Logical '1' level. Therefore, as seen in Figure 1.a, the estimated bits are logical '0' for P_3 condition. It is shown from Figure 1.a that receiver system detects the data bits by taking into account logical level of received signal. In contrast to Figure 1.a, receiver system detects the data bits by using integration of received signal in Figure 1.b. Moreover, the traditional demodulator is used for this condition at the receiver side. The difference between integral values of two slots is the maximum for P_1 condition while it is minimum for P_3 condition. Hence, the bit error rate is maximum for P_3 condition. We gives both hard decision and soft decision expressions under ambient light effect. For soft decision, the received signal is written by

$$x(t) = s(t) + n(t) + y(t), \tag{1}$$

where x(t), s(t), n(t) and y(t) are defined as received signal from output of photodiode, modulated signal, AWGN (Additive White Gaussian Noise) noise and ambient light effect, respectively. The received signal is multiplied by mask signals. Then, output of multiplier is passed through integrator during symbol period. The integration can be expressed by,

$$x_1(t) = K \int_0^{T_S} m_1(t)x(t)d(t), \tag{2}$$

$$x_1(t) = K \int_0^{T_S} m_1(t)(s(t) + n(t) + y(t))d(t) \tag{3}$$

$$x_2(t) = K \int_0^{T_S} m_2(t)x(t)d(t) \tag{4}$$

$$x_2(t) = K \int_0^{T_S} m_2(t)(s(t) + n(t) + y(t))d(t) \tag{5}$$

where K, $m_1(t)$ and $m_2(t)$ are represented as gain and mask signals, respectively. If output of amplifier is equal to saturation value, it must be greater than or equal to $x_1(t)$ and $x_2(t)$. Therefore, the amplifier limits its output to saturation value as shown in Figure 1b. The mask signals can be defined follow as:

$$m_1(t); m_2(t) = \begin{cases} A_m; 0 & 0 < t \le \dfrac{T_S}{2} \\ 0; A_m & \dfrac{T_S}{2} < t \le T_S \end{cases} \tag{6}$$

where A_m represents the amplitude of mask signal. There are two cases related to transmitted symbol: Data bit is logical '1' or '0'. In this paper, we have been analyzed the problem cases taking account both logical '1' and logical '0'.

2.1. The Condition-1. Let Data Bit Be Logical '0'

In this case, we assume that position of pulse is located on the left side of the received signal. Therefore, the Equations (3) and (5) can be written by

$$x_1(t) = A_m K \int_0^{\frac{T_S}{2}} (s(t) + n(t) + y(t))d(t) \tag{7}$$

$$x_2(t) = A_m K \int_{\frac{T_S}{2}}^{T_S} (s(t) + n(t) + y(t))d(t) \tag{8}$$

$$x_1(t) = A_m K \int_0^{\frac{T_S}{2}} (A_s + n(t) + y(t)) d(t) \tag{9}$$

$$x_2(t) = A_m K \int_{\frac{T_S}{2}}^{T_S} (n(t) + y(t)) d(t) \tag{10}$$

where A_s can be described as the amplitude of received signal. As observed in Equation (10), the received signal is zero during the time interval between T_s and $T_s/2$ since the right side of received signal is empty. The Equation (9) can be re-expressed as follows:

$$x_1(t) = \frac{A_m A_s K}{2} + A_m K \int_0^{\frac{T_S}{2}} (n(t) + y(t)) d(t) \tag{11}$$

if the equations analyzed carefully, it will be observed that Equation (10) and the second term of Equation (11) are similar expressions. We assume that ambient light level does not change during the time interval between Ts and $T_s/2$. If ambient light level is defined as A_a, Equations (10) and (11) can be re-written by

$$x_1(t) = \frac{A_m A_s K}{2} + \frac{A_m A_a K}{2} + A_m K \int_0^{\frac{T_S}{2}} n(t) d(t) \tag{12}$$

$$x_2(t) = \frac{A_m A_a K}{2} + A_m K \int_0^{\frac{T_S}{2}} n(t) d(t). \tag{13}$$

2.2. The Condition-2. Let Data Bit Be Logical '1'

This statement expresses that the transmitted bit is being logical '1'. According to this condition, we can re-express Equations (12) and (13) follows:

$$x_1(t) = \frac{A_m A_a K}{2} + A_m K \int_0^{\frac{T_S}{2}} n(t) d(t) \tag{14}$$

$$x_2(t) = \frac{A_m A_s K}{2} + \frac{A_m A_a K}{2} + A_m K \int_0^{\frac{T_S}{2}} n(t) d(t). \tag{15}$$

For both conditions, it is seen that $x_1(t)$ and $x_2(t)$ have similar characteristics. The transmission cannot be provided if the coefficient K of amplifier is adjusted to a proper value by taking account saturation condition. We show this claim as follows:

$$\lim_{K \to K_{sat}} x_1(t) = \lim_{K \to K_{sat}} x_2(t) = x_{sat} \tag{16}$$

where x_{sat} is defined as maximum amplitude at the output of amplifier. Moreover, K_{sat} can be expressed by the minimum gain coefficient which generates the x_{sat}. For hard decision, we give an analysis as follows:

$$C_{1;2} = \frac{1}{2} \sum_{k=1;2}^{N/2;N} \left(\frac{x_{1;2}^k - v}{|x_{1;2}^k - v|} + 1 \right) \tag{17}$$

$$C_d = C_1 - C_2 \tag{18}$$

$$(C_d < 0 \rightarrow d = 0) \land (C_d > 0 \rightarrow d = 1) \tag{19}$$

where the C is defined as number of pulse. The received signal is compared with threshold value to estimate the logical level of received signal. It is determined the number of logical '1' level for two slots. The C_1 presents the number of logical '1' for left half slot while the C_2 gives the number of logical '1' for right half slot. The C_d is applied on comparator to decide data bits. The system is called as slot detector estimation in the reference [23]. In practical systems, the number of logical '1' is affected by clock frequency of FPGA board.

3. TRANSCEIVER SYSTEM

In this section, we give the structure of transceiver system. First, we design a PPM modulator on FPGA board. The PPM signal is generated with respect to data bit. The filled slot is generated at the left slot if data bit is logical '0'. Otherwise, the filled slot is generated at the right slot.

In Figure 2, transceiver model is given for VLC system. As shown in the figure, the modulation process is carried out in Xilinx FPGA board. Afterwards, the modulated signal is emitted through LED (Light Emitted Diode). The signal received from photodiode is a current form. The block converts the signal from current to voltage. In the last stage, the FPGA board is used to estimate the data bits.

The circuit shown in Figure 3 consists of a current to voltage converter and a basic comparator. In the realization of the circuit, single supply quad operational amplifier LM324 is used and the supply voltage is chosen as 3.3 V. The output voltage of the A_1 is linearly related to current which flows on the D photodiode and varied by the light intensity. A_2 is employed as a comparator and produce 3.3 V if the output voltage of A_1 is higher than TH or produce 0 V if it is less then TH.

4. SIMULATION RESULTS

We give the simulation results related to both traditional demodulator and logical level demodulator. The traditional demodulator takes the integral of left and right slots. A comparison is carried out among integral values at the last stage. The data bits are estimated by considering comparison results. Other demodulator is considered as logical level demodulator.

The Figure 4 gives the simulation results for traditional and slot detector. The Ambient Light Effect is shown by using optical power difference between logical '0' and '1'. The ambient light power is increased while the logical '1' level is constant due to saturation of amplifier. Hence, the optical power difference between logical '0' and '1' is decreases if the ambient light power is increased.
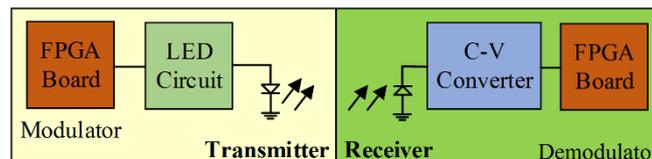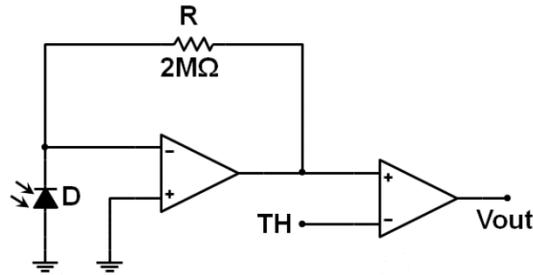

Figure 2. *VLC Transceiver System*

Figure 3. *C-V Converter and Rejection Circuit*
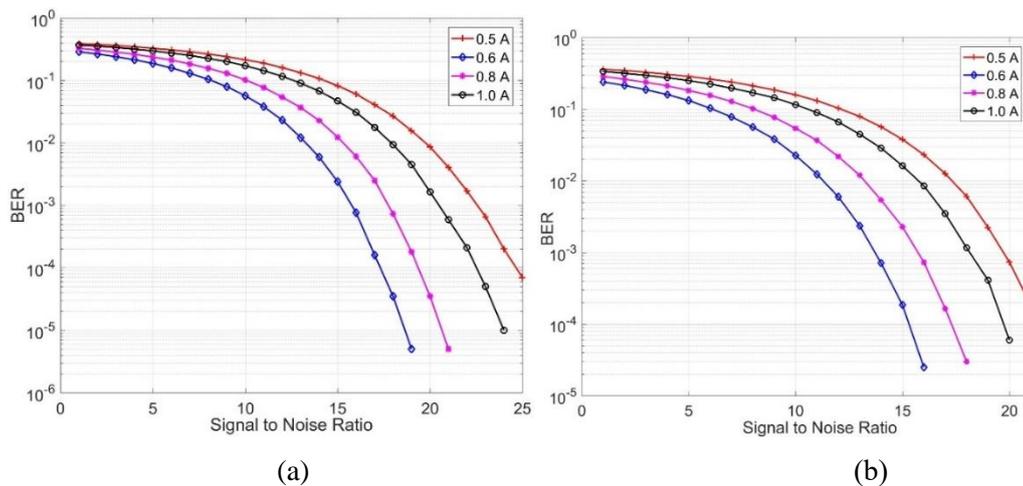

(a)	(b)

Figure 4. *The simulation results (a) hard decision (b) soft decision*

According to simulation results, the A (optical power difference) is decreasing while the BER performance of the system is decreasing. Therefore, the BER performance can be affected from ambient light noise due to amplifier saturation. In saturation region of amplifier for ambient light noise, the logical '1' level is constant while the logical '0' level is increased. The difference between two levels is decreases in this condition. Additionally, the traditional system has better performance than that of slot detector.

5. EXPERIMENTAL RESULTS

In this section, we give the experimental results of system. First, we design a PPM modulator on FPGA board. The PPM signal is generated with respect to data bit. The filled slot is generated at the left slot if data bit is logical '0'. Otherwise, the filled slot is generated at the right slot. In Figure 5, we give PPM modulated signal with respect to data bits.

In Figure 5a, the blue line is defined as modulated PPM signal. As mentioned in previous, the empty and filled slots are determined by using data bits. The data bits are presented by yellow line. In this system, the filled slot is placed at right slot if the transmitted data is logical '1'. Otherwise, the filled slot is generated at left slot as shown in the figure. In Figure 5b, the transmitted and received data is given.
As shown in the Figure 5b, the transmitted data bits are successfully estimated at the receiver side because the ambient light power is very low in this condition.

In Figure 6, we give the structure of experimental transceiver. The Xilinx FPGA is used to provide modulation and demodulation processes. The modulated signal is applied on LED driver by using single pin. Additionally, a single pin is used to receive the output signal of C-V Converter and Rejection Circuit. Hence, we use the demodulator architecture similar as [21].
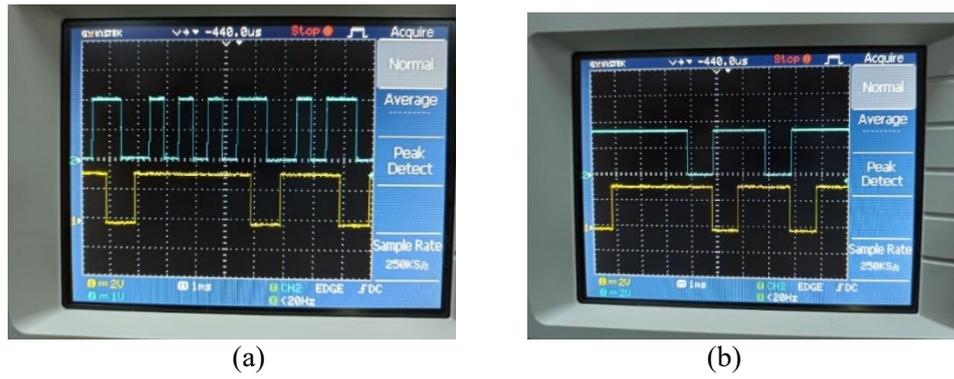
(a)   (b)

Figure 5. *(a) PPM signal with respect to transmitted data signal (b) The transmitted and estimated data bits under low ambient light power*
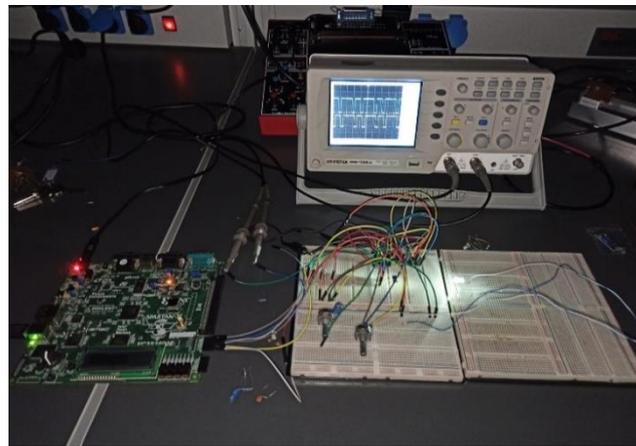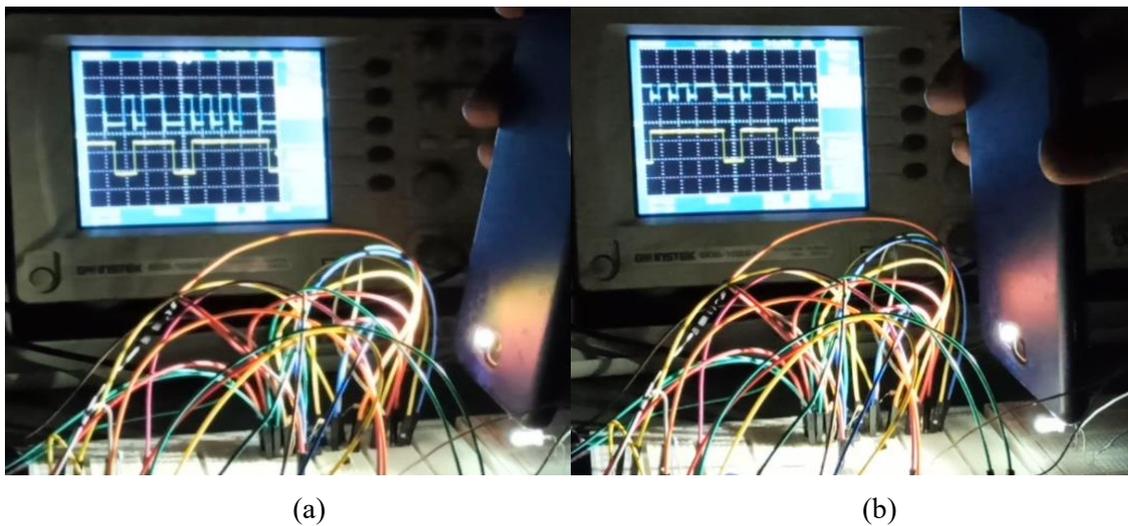

Figure 6. *Transceiver System*

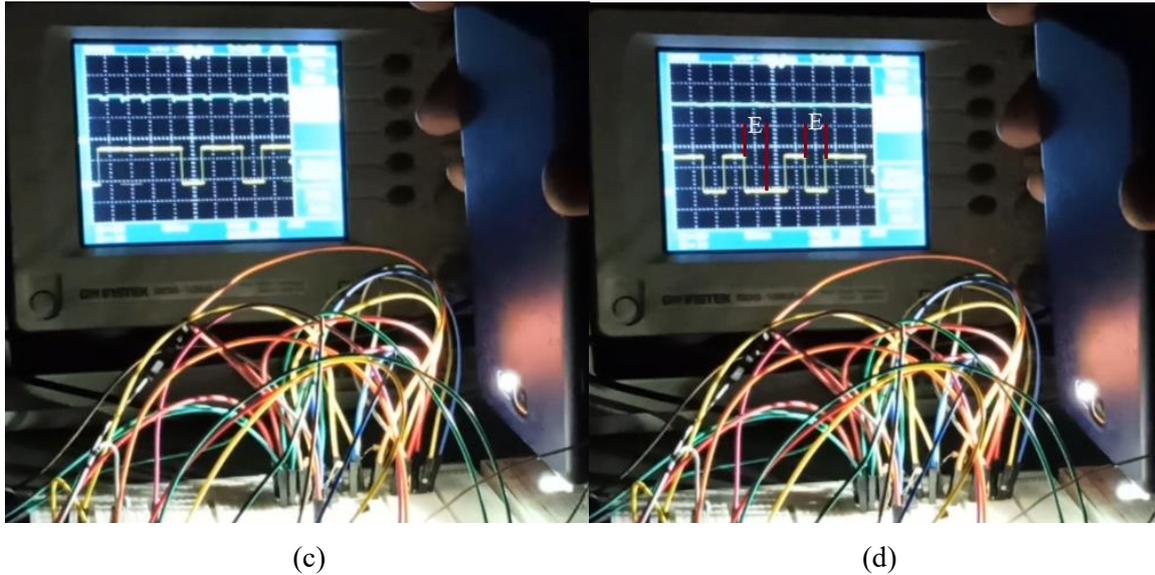(a)   (b)

Figure 7. The performance analysis for various ambient light conditions (a) P1 condition. (b) P2 condition. (c) P3 condition (d) P4 condition

In Figure 7, we give a performance analysis of proposed system. The order of ambient light power on photodiode is P4, P3, P2, and P1. As shown in the Figure 7, the logical '0' of received signal (blue line) is rising while the optical power of ambient light is increasing. The amplitude of logical '1' is approximately 3.3V for all conditions. For Figure 7. a, b, and c, the amplitude of logical '0' is increasing while data bits are successfully estimated. However, the amplitude level of logical '0' is very close to threshold value (TH) in Figure 7.d. Therefore, some bits are error as shown in Figure 7.d. Error bits are defined by using E. By using TH that is presented in Figure 3, the ambient light effect is decreased.

6. CONCLUSION

In this paper, we give a common problem statement for VLC practical systems. The theoretical systems ignore the statement since the system modelling can be difficult. The problem is that amplitude level of logical '1' keeps steady under ambient light due to saturation of C-V output. However, the amplitude level of logical '0' approaches to saturation or logical '1' levels while ambient light power is increasing. Therefore, the detections of logical levels can be difficult. In theoretical systems, a DC can be added to modulated signal instead of ambient light model. This model affects the threshold level of modulated signal. Therefore, it cannot be implemented on PPM systems since the DC is added to all slots. The Empty or Filled Slots can be detected by using integral method. We use a hybrid transceiver for practical system. A Xilinx FPGA and an analog circuit is integrated at the transmitter and the receiver side. This experimental study can be improved by designing and integrating an adaptive gain controller unit to reduce the saturation effect under high power ambient light conditions.

CONFLICTS OF INTEREST

No conflict of interest was declared by the authors.

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