



Research Article

Design and implementation of FPGA-based arrhythmic ECG signals using VHDL for biomedical calibration applications

Fatih Karataş^{a,*} , İsmail Koyuncu^b , Murat Alçın^c  and Murat Tuna^d 

^aAfyon Kocatepe University, Graduate School of Natural and Applied Sciences, Afyonkarahisar 03200, Turkey

^bAfyon Kocatepe University, Faculty of Technology, Department of Electrical and Electronics Engineering, Afyonkarahisar 03200, Turkey

^cAfyon Kocatepe University, Faculty of Technology, Department of Mechatronics, Afyonkarahisar 03200, Turkey

^dKırklareli University, Technical Sciences Vocational High School, Department of Electrical and Energy, Kırklareli 39000, Turkey

ARTICLE INFO

ABSTRACT

Article history:

Received 16 April 2021

Revised 21 June 2021

Accepted 08 July 2021

Keywords:

Arrhythmia

Calibration

ECG

FPGA

Signal Processing

VHDL

Biomedical applications are one of the important research areas of recent years. One of these fields of study is biomedical signals. In this study, the Normal Sinus Rhythm and three arrhythmic ECG signals (Ventricular Tachycardia, Ventricular Paced and Atrial Flutter), one of the vital sign signals, were designed and implemented to work on FPGA chips using the Xilinx-Vivado program with VHDL. Matlab-based ECG signals were taken as a reference and compared with the results obtained from the FPGA-based ECG signals design. Then, the structure used in the design and the test results obtained from the study have been presented. The designed ECG signals were synthesized for the Zynq-7000 XC7Z020 FPGA and observed from the oscilloscope using the 14-channel AN9767 DA module. FPGA chip resource consumption values obtained after the Place-Route process are presented. According to the results, the maximum operating frequency of Normal Sinus Rhythm and Ventricular tachycardia signals on the FPGA was 657.614 MHz and the maximum operating frequency of the Ventricular Paced and Atrial Flutter signals on the FPGA was 651.827 MHz. The maximum MSE value obtained from FPGA-based ECG signal design is 1.2319E-02. In this study, it has been shown that the FPGA-based ECG signal generation system, which is implemented as hardware, can be designed using FPGA chips and can be safely used in biomedical calibration applications. Other arrhythmic ECG signals can be designed and implemented using similar methods in future studies.

1. Introduction

Situations such as heart health, trying to solve problems related to heart health and early diagnosis in every period of life are issues that should be highlighted. One of these issues is Electrocardiography (ECG) and the signals of these values constitute the data groups that should be followed in the first place about the patient [1].

Calibration is a series of measurements used to measure the accuracy, determine and document deviations of another test and measuring instrument using a measurement standard or system of known accuracy under specified conditions. The importance of calibration becomes clearer if we estimate what it will cost in a sector that is difficult to return, such as health, because a medical device that makes an erroneous measurement adversely

affects the diagnostic process. With calibration: The accuracy of all measurements performed is ensured. Production quality is increased to the desired level. Any deviations and errors that may arise during the production stages are detected and corrected in advance. It is ensured that the products are compatible with other company products. The possibility of competition increases. The opportunity to catch and use advanced technology is provided. The manufactured product is in compliance with international standards. Unfair profit from the customer or gaining unfair advantage to the customer is prevented. Our health is evaluated with correct diagnosis and treatment opportunities. All devices used in health institutions must be subjected to a calibration process within certain periods. The devices used for this purpose are called medical calibrator devices. The calibrator whose design is

* Corresponding author. Tel.: +90-272- 218-14-60; Fax: +90-272- 218-14-62.

E-mail addresses: fatihkaratas@usr.aku.edu.tr (F. Karataş), ismailkoyuncu@aku.edu.tr (İ. Koyuncu), muratalcin@aku.edu.tr (M. Alçın), murattuna@klu.edu.tr (M. Tuna)

ORCID: 0000-0003-1877-5552 (F. Karataş), 0000-0003-4725-4879 (İ. Koyuncu), 0000-0002-2874-7048 (M. Alçın), 0000-0003-3511-1336 (M. Tuna)

DOI: 10.35860/iarej.918874

© 2021, The Author(s). This article is licensed under the CC BY-NC 4.0 International License (<https://creativecommons.org/licenses/by-nc/4.0/>).

mentioned in this study is the ECG Simulator [2].

Field Programmable Gate Arrays (FPGA) are widely accepted in medical systems due to their capabilities such as rapid prototyping, reprogramming, parallel processing and high performance of a concept that requires co-design as hardware or software [3].

Very successful studies are carried out with FPGA chips in the field of signal processing using digital hardware [4].

In the literature, the signals used in the studies of the ECG and vital signs signals on FPGA chips: These are analog signals recorded with medical devices such as ECG, patient monitor, or rhythm holer [5].

Hundreds of signal samples taken at various times from people with different types of ailments in different regions were used from national/international databases [6].

Studies conducted in this area are generally in the form of taking ECG signals from databases, which were previously recorded from the patient, non-artificial, real signals and applying them to FPGA chips with the help of Analog Digital Converter (ADC) and Digital Analog Converter (DAC) [7]. Studies on these signals received from the patient; Heart rate calculation [8], detection of rhythm disturbances [9], detection of peak on the signal [10], normalization of noisy ECG signals by applying filters such as Finite Impulse Response (FIR) [11], Quadrature Mirror Filters (QMF) and Infinite Impulse Response (IIR) [12], ECG signal filtering in FPGA [13], classification of ECG signals with the Discrete Wavelet Transform (DWT) method for the detection of the QRS (The three graphs (Q wave, R wave, and S wave) found in a typical ECG are a combination of the deviation) complex [14].

ECG Simulators are commonly performed with microcontrollers [15–20]. However, these do not work in parallel like FPGA chips, they work in series.

As can be seen in the literature research, the studies of vital signs and ECG signals using FPGA technology are in the form of recording these signals from the human body through a medical device, storing them in databases and taking them from there and using them if needed.

In this study, four ECG signals (Normal Sinus Rhythm, Ventricular Tachycardia, Ventricular Paced and Atrial Flutter) are modeled by presenting a new approach on FPGA [21]. In the first place, ECG signals were mathematically designed and observed in Matlab. Then, ECG signals have been modeled for using in FPGA chips in Xilinx-Vivado with Very High-Speed Integrated Circuits (VHSIC) Hardware Description Language (VHDL), which is a structural hardware description language. After that, these signals were compared with Matlab-based signals and the error values obtained from the comparison were presented. Information was given about the FPGA chip and DAC used in the design. Oscilloscope images of the obtained signals are shown.

The working frequencies of the FPGA-based ECG signal generation system and the chip statistics obtained from the design are presented. In the second part of the study, information about ECG signals, FPGA chips and system components are given. In the third part, FPGA-based ECG signal design and FPGA chip statistics obtained from the design are given. In the last part, the results obtained from the design are evaluated.

2. Background Information

2.1 ECG Signal

The process of recording and interpreting the systole and diastole phases of the atrium and ventricles of the heart, the electrical activity that occurs during the stimulation and transmission of the heart on a moving millimeter paper by magnifying the electrical potential created by the heart tissue is called Electrocardiography, the recording device is called Electrocardiograph and the signal obtained is called Electrocardiogram [22].

This Non-invasive method has been developed to examine the operation of the heart muscle and the neural conduction system of the heart, to diagnose and then to apply the correct treatment, heart enlargement, reduction in the amount of blood to the heart, observation of problems in the heart valves, new or old heart damage, heart rhythm problems. Also, it can provide important information about many cardiac and pericardial diseases that carry the risk of premature death. Therefore, ECG, signal processing and modeling are considered as some of the most important issues in biomedical applications [23].

ECG signal; It is a normal sinus rhythm as shown in Figure 1 consisting of waves, segments and intervals. Waves; P, Q, R, S, T and U wave. Segments; PR-Segment and ST-Segment. Intervals; QT-interval, PR-interval, RR-interval. These values vary in arrhythmic signals [24]. In this study, Normal Sinus Rhythm (NSR) and three arrhythmic ECG signals (Ventricular Tachycardia, Ventricular Paced and Atrial Flutter) were used as a reference in FPGA design. NSR is shown in Figure 2, Ventricular Tachycardia in Figure 3, Ventricular Paced in Figure 4, and Atrial Flutter in Figure 5, respectively [25].

2.2 Development FPGA Board and System Components

FPGAs are digital Integrated Circuits (IC) with re-programmable features, whose hardware structure can be changed by the user/designer according to the desired function after production. It stands out with its features such as parallel processing, low power consumption, rapid initial prototyping, high operating frequency and high performance compared to other platforms [26]. FPGA chips can be programmed in coding languages such as VHDL, Verilog, Handel-C and System C [27].

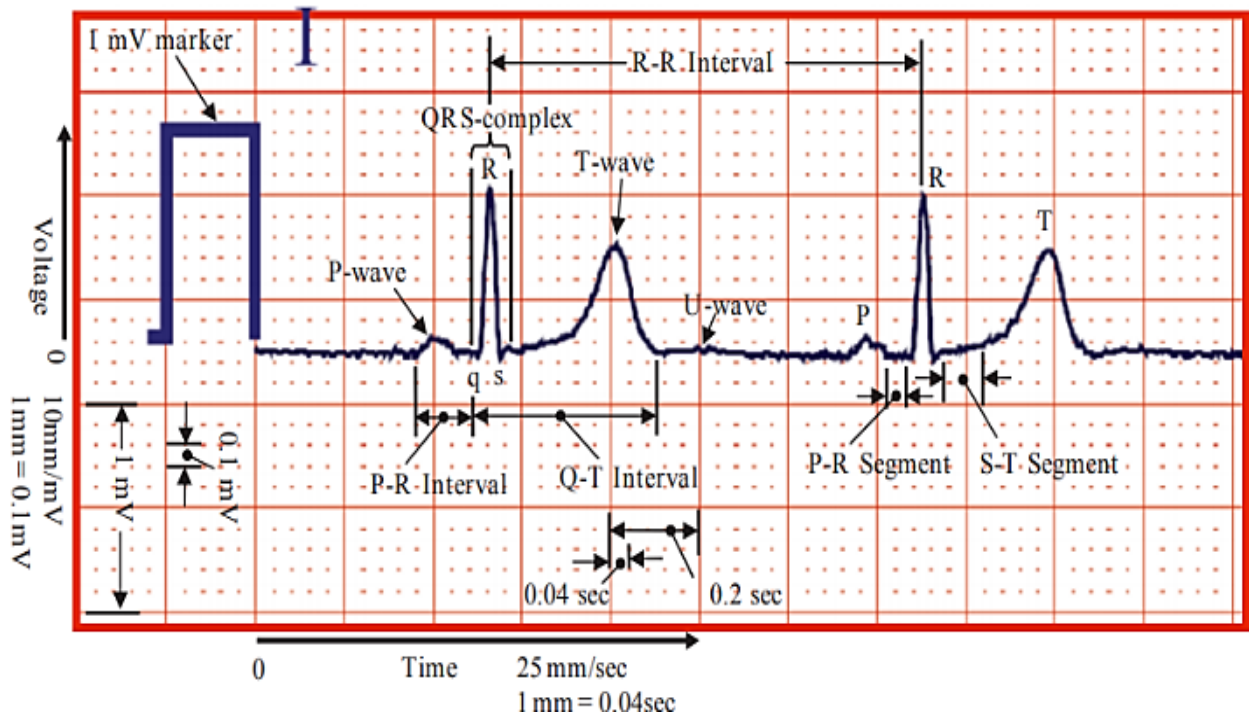


Figure 1. Typical ECG of a normal person



Figure 2. Normal Sinus Rhythm (NSR)



Figure 4. Ventricular Paced



Figure 3. Ventricular Tachycardia

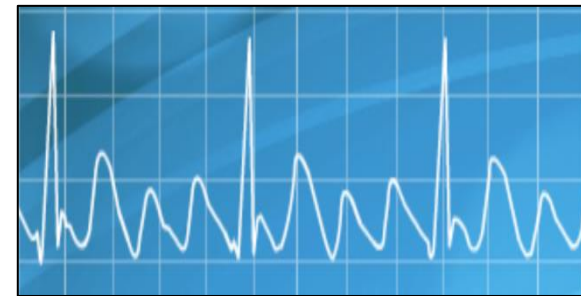


Figure 5. Atrial Flutter

An FPGA consists of three programmable components: configurable logic blocks (CLB), input-output blocks (IOB) and interconnection networks. It consists of various elements such as Look-Up Table (LUT) where logical functions can be created, Flip-Flops where single-bit information can be stored and Multiplexers that direct the information flow. Figure 6 shows the FPGA components [28].

FPGA chips are widely used in many areas in recent years. These working areas are; Artificial Neural Networks (ANN) [29], fuzzy logic applications [30], chaotic oscillator design

[31], Pseudo and True Random Number Generators [32], robotics [33], space, aviation and defense industry [34], purpose-built integrated prototypes such as Application Specific Integrated Circuit (ASIC), audio, automotive industry, press and media, consumer electronics, data center, high-performance computing and data storage industry, video and image processing, wired/wireless communication, biomedical applications and medical devices [35-39].

This study was carried out using the Zynq-7000 SoC XC7Z020 FPGA development board shown in Figure 7 and the 14-bit AN9767 DAC module shown in Figure 8.

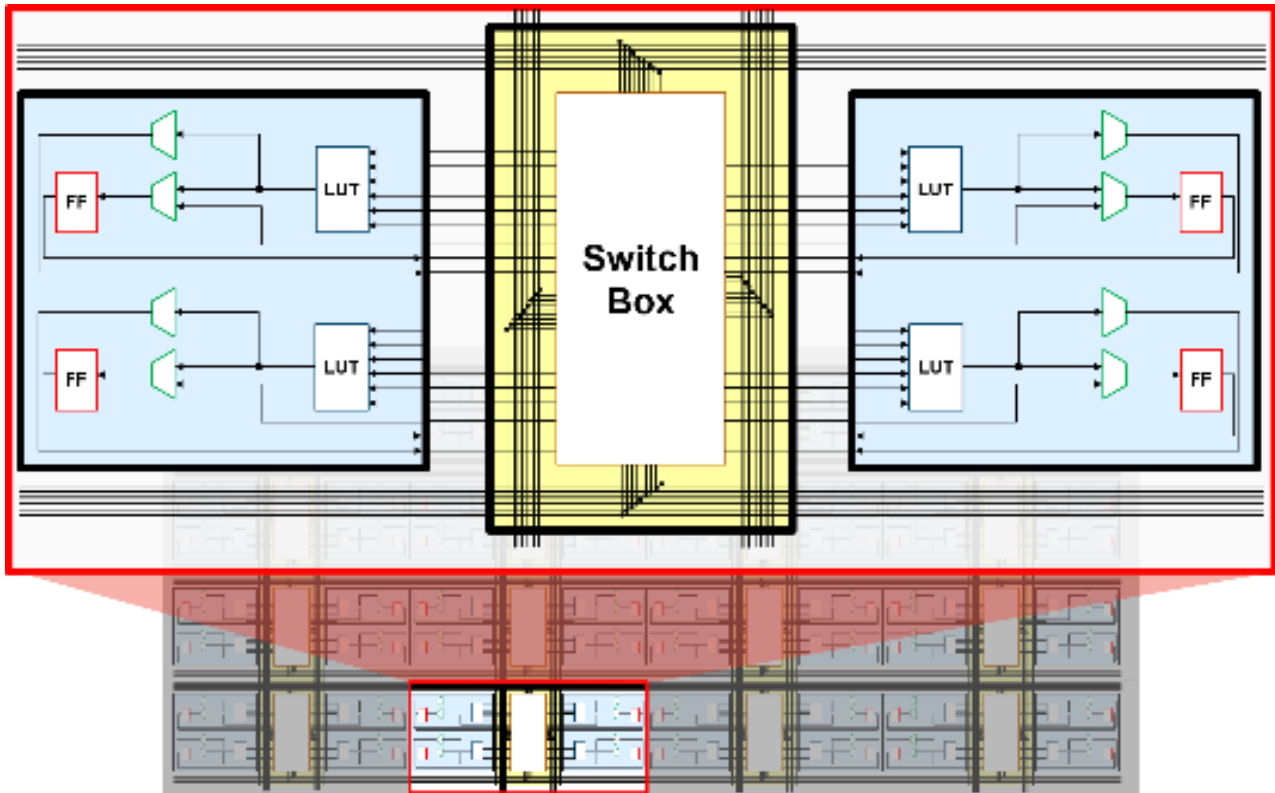


Figure 6. FPGA architecture

The AX7020 FPGA development board uses Xilinx's Zynq7000 series of chips, model XC7Z020-2CLG400I, in a 40-pin FPGA package. The ZYNQ7000 chip can be divided into a Processor System part (PS) and a Programmable Logic part (PL). On the AX7020 development board, the PS and PL sections of the ZYNQ7000 are equipped with a wealth of external interfaces and devices for user convenience and functional verification [40].

3. FPGA-based design of ECG Signals

The system is designed as a block that generates an ECG signal according to parameters in Xilinx-Vivado software using VHDL. The working logic of the system as follows; The results of the mathematical equations created within the scope of the study (functions that calculate ECG values) are recorded in LUTs (Look-Up Table). Then, by creating a phase register, the phase register increases with every rising clock signal and this increased value is modeled to load the values in the LUT and transfer them to the output. This situation is repeated in each period during the clock.

Firstly, Normal Sinus Rhythm (NSR) with 72 bpm heart rate, Ventricular Tachycardia signal with 210 bpm heart rate, Ventricular Paced signal with 75 bpm heart rate and Atrial Flutter signal with 150 bpm heart rate have been modeled in Matlab in accordance with time and amplitude values. The NSR signal modeled in Matlab is shown in Figure 9, the Ventricular Tachycardia signal in Figure 10, the Ventricular Paced signal in Figure 11, and the Atrial Flutter signal in Figure 12.



Figure 7. ALINX AX7020: Zynq-7000 SoC XC7Z020 FPGA Development Board

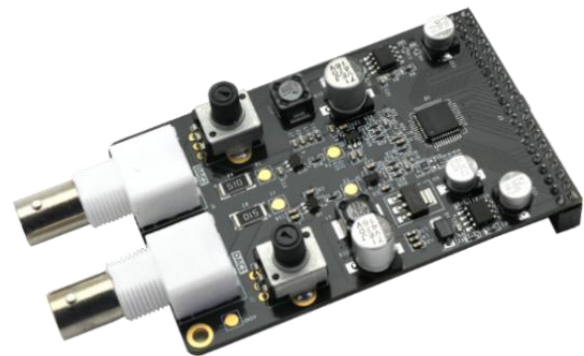


Figure 8. 14-bit Dual Port DAC Output Module AN9767

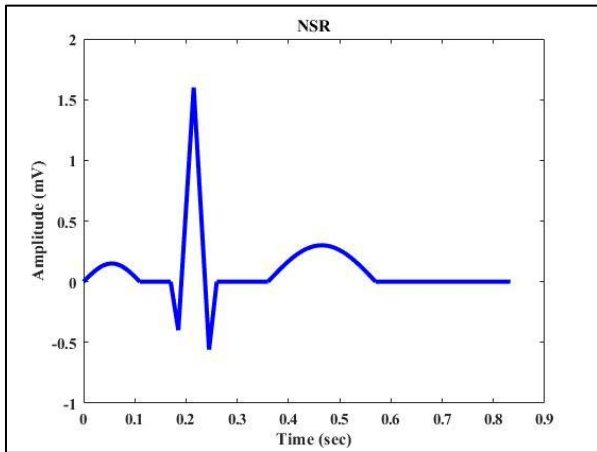


Figure 9. Normal Sinus Rhythm (NSR) with 72 bpm heart rate in Matlab

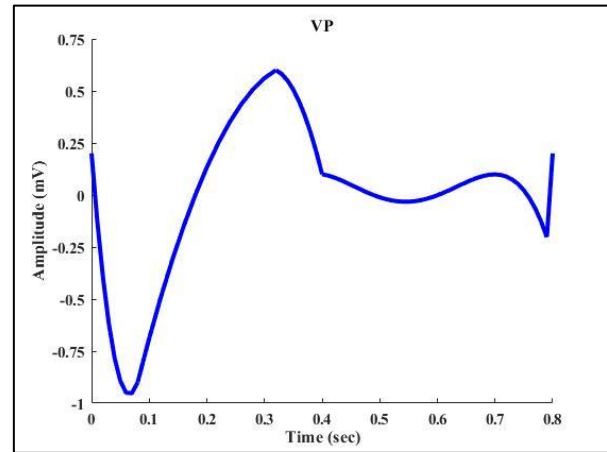


Figure 11. Ventricular Paced signal with 75 bpm heart rate in Matlab

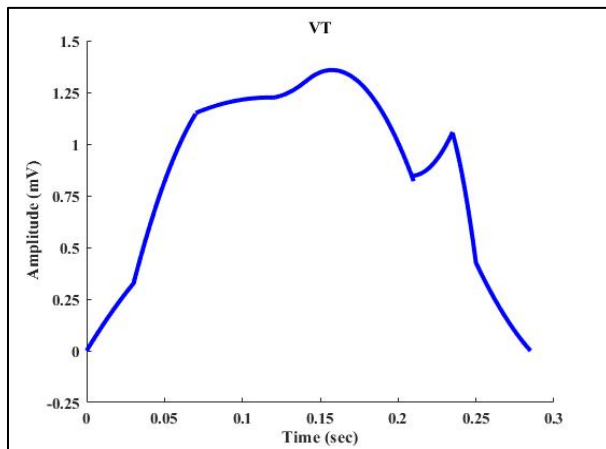


Figure 10. Ventricular Tachycardia signal with 210 bpm heart rate

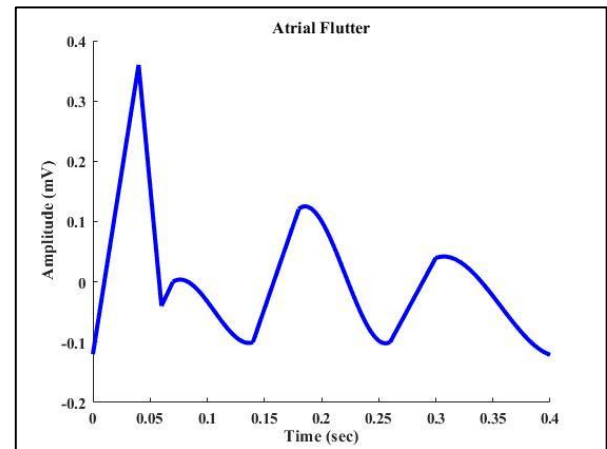


Figure 12. Atrial Flutter signal with 150 bpm heart rate in Matlab

The mathematical equation of the P wave generation of the ECG signal, which is called Normal Sinus Rhythm and whose heart rate is designed as 72 bpm per minute, is shown in Equation (1) in Table 1. In addition, the generations of PR-segment, QRS complex, ST-segment and T wave are illustrated in Equation (2), Equation (3), Equation (4) and Equation (5), respectively. The stationary period from the last part of the T wave to the beginning of the P wave of the next ECG signal is given in Equation (6). The amplitude and time parameters of the NSR are shown in Table 2 and Table 3, respectively.

Then, these four ECG signals were designed in the Xilinx-Vivado program using VHDL. The signals observed on the Vivado simulation screen, namely the NSR signal, are shown in Figure 13, the Ventricular Tachycardia signal in Figure 14, the Ventricular Paced signal in Figure 15, and the Atrial Flutter signal in Figure 16.

The first-order block diagram of the top module of the FPGA-based ECG signal generation system designed to operate on the FPGA chip is given in Figure 17. The second-order block diagram of the system for NSR and the block producing the ECG Signal are given in Figure 18.

Table 1. Mathematical equations for the NSR designed in Matlab

| | |
|--|-----|
| $x_1 = 0:0.005:p_int$ $y_1 = p_peak * \sin(x_1 * \frac{\pi}{p_int})$ | (1) |
| $x_2 = p_int:0.01:pr_int$ $y_2 = 0 * x_2$ | (2) |
| $q_1 = pr_int + 0.015$ $x_3 = pr_int:0.005:q_1$ $y_3(Q\ wave) = -26.667 * x_3 + 4.53333$ $r_1 = pr_int + 0.045$ $x_4 = q_1:0.005:r_1$ $y_4(R\ wave) = 66.667 * x_4 - 12.733$ $s_1 = pr_int + 0.075$ $x_5 = r_1:0.005:s_1$ $y_5(S_1\ wave) = -72 * x_5 + 17.08$ $s_2 = pr_int + qrs_int$ $x_6 = s_1:0.005:s_2$ $y_6(S_2\ wave) = 37.333 * x_6 - 9.706$ | (3) |
| $t_1 = pr_int + qrs_int + st_seg$ $x_7 = s_2:0.01:t_1$ $y_7 = 0 * x_7$ | (4) |
| $t_2 = pr_int + qt_int$ $x_8 = t_1:0.005:t_2$ $y_8 = t_peak * \sin((x_8 - t_1) * \frac{\pi}{t_2 - t_1})$ | (5) |
| $delay = h - t_2$ $x_9 = t_2:0.01:h$ $y_9 = 0 * x_9$ | (6) |

Table 2. Amplitude parameters of NSR

| NSR parameters | Amplitude (mV) |
|-----------------|----------------|
| P wave (p_peak) | 0.15 |
| Q wave (q_peak) | 0.40 |
| R wave (r_peak) | 1.60 |
| S wave (s_peak) | 0.56 |
| T wave (t_peak) | 0.30 |

Table 3. Time parameters of NSR

| NSR parameters | Time (sec.) |
|-----------------------|-------------|
| P wave (p_int) | 0.11 |
| PR-interval (pr_int) | 0.17 |
| PR-segment (pr_seg) | 0.06 |
| ST-segment (st_seg) | 0.10 |
| QT-interval (qt_int) | 0.40 |
| QRS complex (qrs_int) | 0.09 |
| T wave (t_int) | 0.21 |

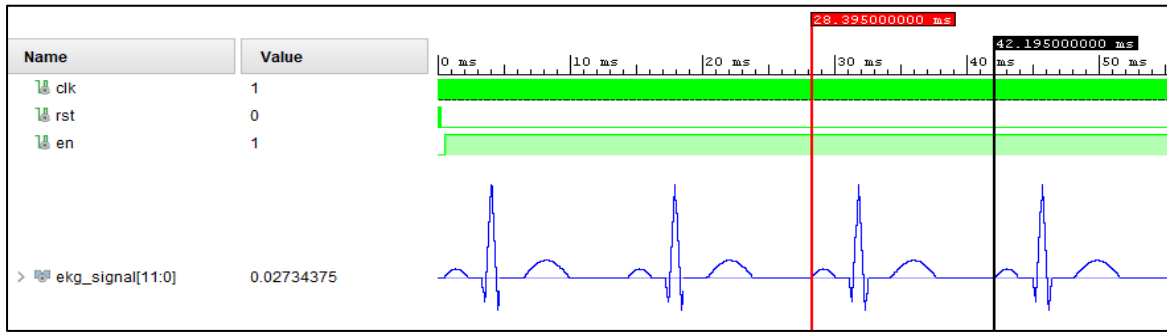


Figure 13. Vivado Simulation of NSR

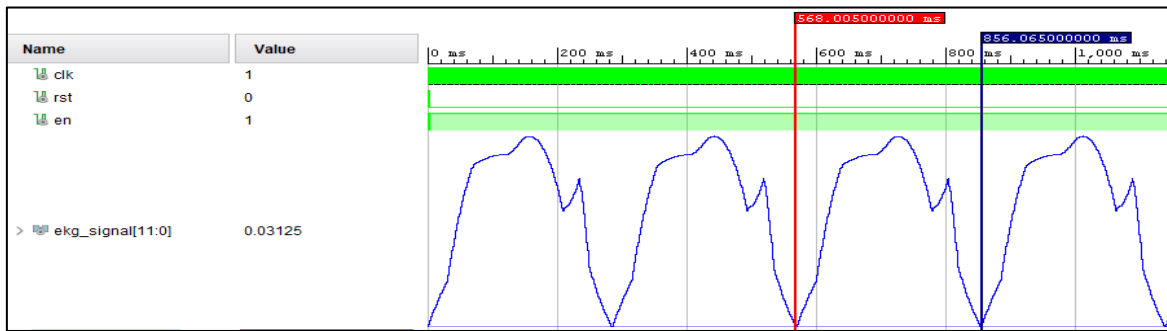


Figure 14. Vivado Simulation of Ventricular Tachycardia

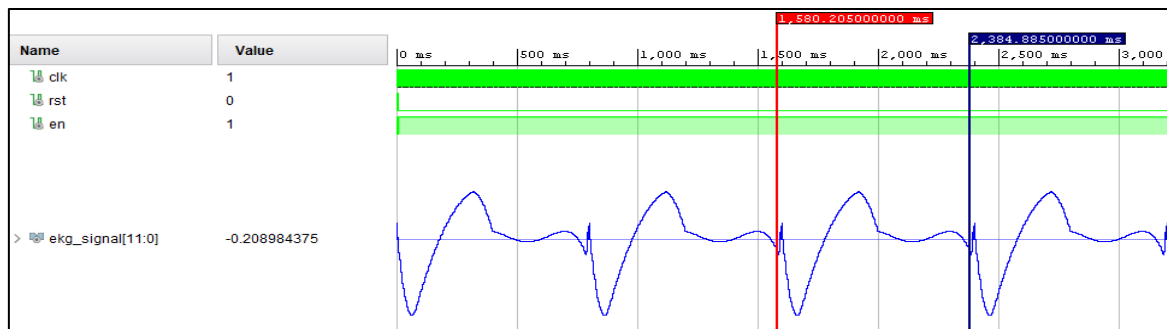


Figure 15. Vivado Simulation of Ventricular Paced



Figure 16. Vivado Simulation of Atrial Flutter

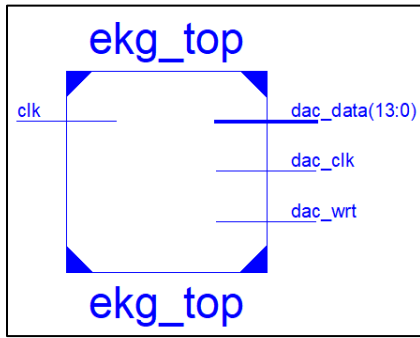


Figure 17. The first-order block diagram of the system top module

The designed ECG signals were synthesized for Zynq-7000 XC7Z020 FPGA and observed over the

oscilloscope using the 14-channel AN9767 DA module. The NSR signal observed from the oscilloscope is given in Figure 19, the Ventricular Tachycardia signal in Figure 20, the Ventricular Paced signal in Figure 21, and the Atrial Flutter signal in Figure 22, respectively.

Matlab-based ECG signals were taken as a reference and compared with the results obtained from the FPGA-based ECG signals design and this comparison is shown in Table 4. As a result of this comparison, the maximum MSE value for the NSR signal obtained from the FPGA-based ECG signal design is 1.2319E-02, the MSE value for the Ventricular Tachycardia signal is 8.5333E-07, the MSE value for the Ventricular Paced signal is 2.9538E-05, and the Atrial Flutter MSE value is 3.3255E-03.

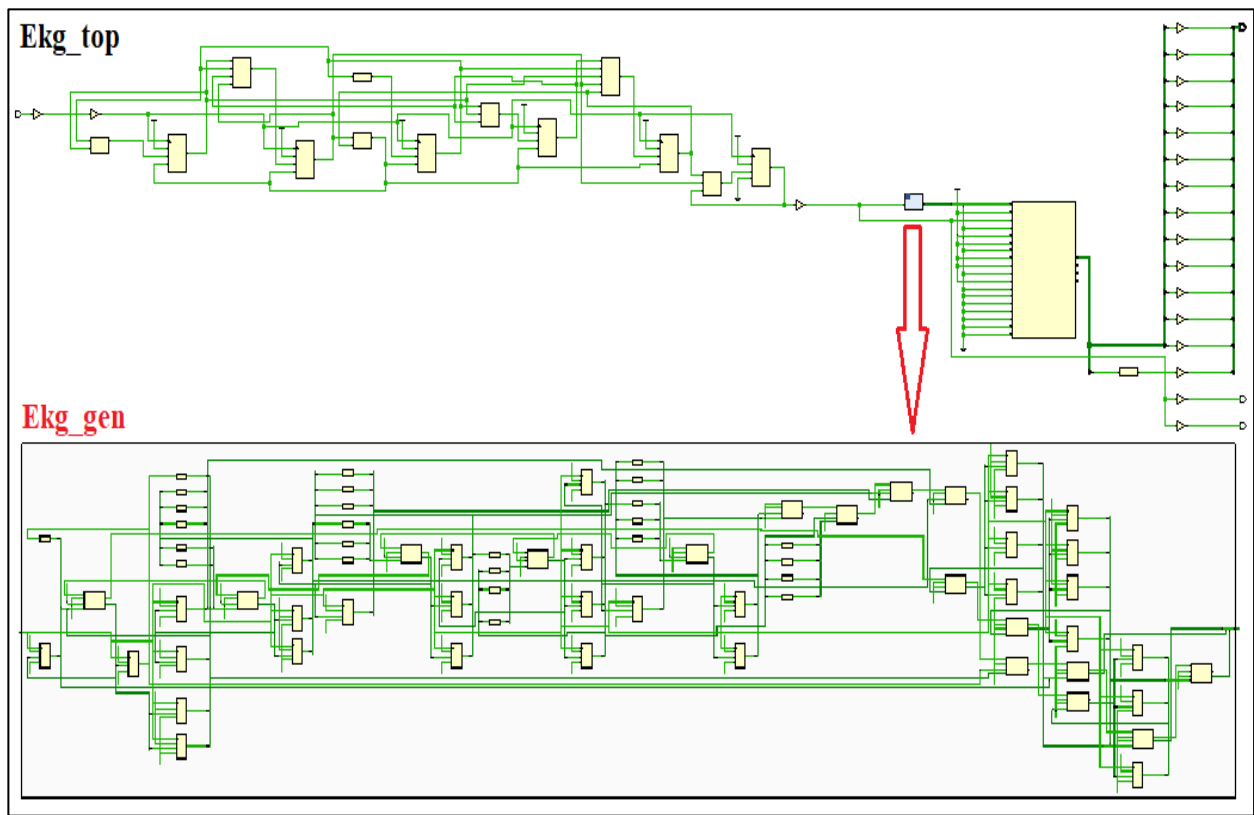


Figure 18. The second-order block diagram of the system for NSR and the block generating the ECG Signal



Figure 19. NSR observed on oscilloscope



Figure 20. Ventricular Tachycardia observed on oscilloscope



Figure 21. Ventricular Paced observed on oscilloscope



Figure 22. Atrial Flutter observed on oscilloscope

The usage statistics for the Zynq-7000 chip of the FPGA-based ECG signal generation system obtained after the Place-Route process are given in Table 5. According to the results, the maximum operating frequency of NSR and VT signals on FPGA was determined as 657.614 MHz. The maximum operating frequency of VP and Atrial Flutter on FPGA has been determined as 651.827 MHz.

4. Conclusions

In this study, Normal Sinus Rhythm, one of the vital signs for biomedical calibration applications and three arrhythmic ECG signals (Ventricular Tachycardia, Ventricular Paced and Atrial Flutter) were designed and implemented to work on FPGA chips using the Xilinx-Vivado program with VHDL. These signals were first mathematically modeled in Matlab and the accuracy of the obtained graphics was compared and evaluated in accordance with the literature. Later, in the Xilinx-Vivado program, using VHDL, the verified signals in Matlab were designed. Matlab-based ECG signals were taken as a reference and compared with the results obtained from the FPGA-based ECG signals design. As a result of this comparison, the maximum MSE value obtained from the FPGA-based ECG signal design is 1.2319E-02. The designed ECG signals were synthesized for Zynq-7000 XC7Z020 Alinx FPGA and observed from the oscilloscope using the 14-channel AN9767 DAC module. FPGA chip resource consumption values obtained after the Place-Route process are presented.

Table 4. The comparison of Normal Sinus Rhythm in Matlab and Vivado

| NSR | Time (sec.) | | Amplitude (mV) | |
|-------------------|-----------------|----------|----------------|----------|
| | Matlab & Vivado | | Matlab | Vivado |
| P wave | 0.00000 | 0.00000 | 0.00000 | 0.00000 |
| | 0.00500 | 0.02135 | 0.02148 | 0.02148 |
| | 0.01000 | 0.04225 | 0.04101 | 0.04101 |
| | 0.02000 | 0.08109 | 0.08007 | 0.08007 |
| | 0.03000 | 0.11336 | 0.11328 | 0.11328 |
| | 0.03500 | 0.12618 | 0.12695 | 0.12695 |
| | 0.04000 | 0.13644 | 0.13671 | 0.13671 |
| | 0.04500 | 0.14392 | 0.14453 | 0.14453 |
| | 0.05000 | 0.14847 | 0.14843 | 0.14843 |
| | 0.05500 | 0.15000 | 0.15039 | 0.15039 |
| | 0.06000 | 0.14847 | 0.14843 | 0.14843 |
| | 0.07000 | 0.13644 | 0.13671 | 0.13671 |
| | 0.08000 | 0.11336 | 0.11328 | 0.11328 |
| | 0.09000 | 0.08109 | 0.08007 | 0.08007 |
| | 0.09500 | 0.06231 | 0.06445 | 0.06445 |
| | 0.10000 | 0.04225 | 0.04101 | 0.04101 |
| | 0.10500 | 0.02134 | 0.02148 | 0.02148 |
| | PR segment | 0.11000 | 0.00183 | 0.00000 |
| 0.17000 | | 0.00000 | 0.00000 | 0.00000 |
| QRS wave | 0.17500 | -0.13339 | -0.13281 | -0.13281 |
| | 0.18000 | -0.26673 | -0.26367 | -0.26367 |
| | 0.18500 | -0.40006 | -0.41796 | -0.41796 |
| | 0.20000 | 0.60040 | 0.61328 | 0.61328 |
| | 0.20500 | 0.93373 | 0.93945 | 0.93945 |
| | 0.21000 | 1.26707 | 1.26367 | 1.26367 |
| | 0.22000 | 1.24000 | 1.25976 | 1.25976 |
| | 0.23000 | 0.52000 | 0.49804 | 0.49804 |
| | 0.23500 | 0.98800 | 0.96679 | 0.96679 |
| | 0.24000 | -0.20000 | -0.20507 | -0.20507 |
| | 0.25000 | -0.37270 | -0.37890 | -0.37890 |
| | 0.25500 | -0.18610 | -0.19726 | -0.19726 |
| ST segment | 0.26000 | 0.00000 | 0.00000 | 0.00000 |
| | 0.36000 | 0.00000 | 0.00000 | 0.00000 |
| T wave | 0.37000 | 0.04470 | 0.42968 | 0.42968 |
| | 0.39000 | 0.13020 | 0.12890 | 0.12890 |
| | 0.41000 | 0.20410 | 0.20507 | 0.20507 |
| | 0.42000 | 0.23450 | 0.23437 | 0.23437 |
| | 0.44000 | 0.27930 | 0.27929 | 0.27929 |
| | 0.45000 | 0.29250 | 0.29296 | 0.29296 |
| | 0.46000 | 0.29920 | 0.29882 | 0.29882 |
| | 0.47000 | 0.29920 | 0.29882 | 0.29882 |
| | 0.48000 | 0.29250 | 0.29296 | 0.29296 |
| | 0.50000 | 0.25980 | 0.25976 | 0.25976 |
| | 0.51000 | 0.23450 | 0.23437 | 0.23437 |
| | 0.52000 | 0.20410 | 0.20312 | 0.20312 |
| | 0.53000 | 0.16900 | 0.16992 | 0.16992 |
| | 0.54000 | 0.13200 | 0.13281 | 0.13281 |
| | 0.55000 | 0.08840 | 0.08789 | 0.08789 |
| Stationary period | 0.56000 | 0.04470 | 0.04492 | 0.04492 |
| | 0.57000 | 0.00000 | 0.00000 | 0.00000 |
| | 0.83000 | 0.00000 | 0.00000 | 0.00000 |

According to the results, the maximum operating frequency of Normal Sinus Rhythm and Ventricular tachycardia signals on the FPGA was 657.614 MHz and the maximum operating frequency of the Ventricular Paced and Atrial Flutter signals on the FPGA was 651.827 MHz. With this study, it has been shown that the hardware designed FPGA-based ECG signal generation system can be designed using FPGA chips, can be utilized safely in biomedical calibration applications and can be used in ECG Simulators used for calibration tests of medical devices in the field of cardiology.

Table 5. The usage statistics for the Zynq-7000 chip of FPGA based ECG signal generation system

| Logic Utilization / Usage rate | NSR | Ventricular Tachycardia | Ventricular Paced | Atrial Flutter |
|-----------------------------------|-------------|-------------------------|-------------------|----------------|
| Number of BUFGCTLs | 2 / %6.25 | 2 / %6.25 | 2 / %6.25 | 2 / %6.25 |
| Number of Slice LUTs | 39 / %0.073 | 39 / %0.073 | 40 / %0.075 | 40 / %0.075 |
| Number of Slice Registers | 38 / %0.035 | 38 / %0.035 | 39 / %0.036 | 39 / %0.036 |
| Maximum Operating Frequency (MHz) | 657.614 | 657.614 | 651.827 | 651.827 |
| Mean Squared Error (MSE) | 1.2319E-02 | 8.5333E-07 | 2.9538E-05 | 3.3255E-03 |

In future studies, other arrhythmic ECG signals can be modeled using similar methods and also vital sign signals such as SPO₂, ETCO₂ and blood pressure can be added to increase the variety of signals to be used for calibration.

Declaration

The author(s) declared no potential conflicts of interest with respect to the research, authorship and/or publication of this article. The author(s) also declared that this article is original, was prepared in accordance with international publication and research ethics and ethical committee permission or any special permission is not required.

Author Contributions

All the authors have equally contributed.

Acknowledgment

This study is sponsored by the Scientific and Technological Research Council of Turkey (TUBITAK) with project number 119E659.

References

- Do Vale Madeiro, J.P., Cortez, P.C., Salinet, J.L., Pedrosa, R.C., da Silva Monteiro Filho, J.M., and Brayner, A.R.A., *Classical and Modern Features for Interpretation of ECG Signal*, Developments and Applications for ECG Signal Processing: Modeling, Segmentation, and Pattern Recognition, Elsevier, 2019. p. 1–28.
- Yang, S., Lam, B., and Ng, C.M.N., *Calibration of Electrocardiograph (ECG) Simulators*. NCSLI Measure, 2018. **12**(1): p. 46–53.
- Koyuncu, İ., Özcerit, A.T., Pehlivan, İ., and Avarođlu, E., *Design and implementation of chaos based true random number generator on FPGA*. In 2014 22nd IEEE Signal Processing and Communications Applications Conference, 2014. p. 236–239.
- Meyer-Base, U., *Introduction., Digital Signal Processing with Field Programmable Gate Arrays*, Berlin, Heidelberg, 2014. p. 1–52.
- Life in the fast lane. *ECG Library Basics*. [cited 2021 11 February]; Available from: <https://litfl.com/ecg-library/>.
- PhysioNet. *The research resource for complex physiologic signals. Physio Bank ATM, MIT, and BIH Arrhythmia Database*. [cited 2021 11 February]; Available from: <https://archive.physionet.org/>.
- Kumar, S., Singh, G., and Kaur, M., *FPGA Implementation of Electrocardiography (ECG) Signal Processing 1*. An International Journal of Engineering Sciences, 2016. p. 2229–6913.
- Desai, V., *Electrocardiogram (ECG/EKG) using FPGA*, San Jose State University, Computer Science, Master's Thesis, USA, 2012. p. 11-15.
- Madiraju, N.S., Kurella, N., and Valapudasu, R., *FPGA Implementation of ECG Feature Extraction Using Time Domain Analysis*. Electrical Engineering and Systems Science, Signal Processing (eess.SP); Hardware Architecture (cs.AR), 2018. arXiv:1802.03310
- Agrawal, A., and Gawali, D.H., *FPGA-Based Peak Detection of ECG Signal Using Histogram Approach*, International Conference on Recent Innovations in Signal Processing and Embedded Systems, RISE 2017, Institute of Electrical and Electronics Engineers Inc., 2017. p. 463–468.
- Alhelal, D., and Faezipour, M., *Denoising and Beat Detection of ECG Signal by Using FPGA*. International Journal of High Speed Electronics and Systems, 2017. **26**(3): p. 1740016.
- Su, W., Liang, Y., Li, M., and Li, Y., *The Research and FPGA Implementation of ECG Signal Preprocessing*, International Conference on Biomedical and Health Informatics, IFMBE Proceedings, Springer Verlag, Singapore, 2018. p. 167–168.
- Popa, R., *ECG Signal Filtering in FPGA*, 2019 6th International Symposium on Electrical and Electronics Engineering, ISEEE 2019, Galati, Romania, 2019. p. 1-6.
- Egila, M.G., El-Moursy, M.A., El-Hennawy, A. E., El-Simary, H.A., and Zaki, A., *FPGA-Based Electrocardiography (ECG) Signal Analysis System Using Least-Square Linear Phase Finite Impulse Response (FIR) Filter*. Journal of Electrical Systems and Information Technology, 2016. **3**(3): p. 513–526.
- Shirzadfar, H., and Khanahmadi, M., *Design and Development of ECG Simulator and Microcontroller Based Displayer*. Journal of Biosensors & Bioelectronics, 2018. **9**(3): p. 1–9.
- Cho, S., Lee, Y., and Chang, I., *Designing a Novel ECG Simulator: Multi-Modality Electrocardiography into a Three-Dimensional Wire Cube Network*. IEEE Technology and Society Magazine, 2016. **35**(1): p. 75–84.
- Paul, A.D., Urzoshi, K.R., Datta, R.S., Arsalan, A., Azad, A.M., *Design and Development of Microcontroller Based ECG Simulator*, In: Osman, N.A.A., Abas, W.A.B.W., Wahab, A.K.A., Ting, HN. (eds) 5th Kuala Lumpur International Conference on Biomedical Engineering, IFMBE Proceedings, Berlin, Heidelberg, 2011. **35**: p. 292-295.
- Jun-an, Z., *The Design of ECG Signal Generator using PIC24F*, Procedia Engineering, International Conference on Advances in Engineering, 2011. **24**: p. 523-527.
- Chien, J.R.C., *Design of a Programmable Electrocardi-*

- ogram Generator Using a Microcontroller and the CPLD Technology, IECON Proceedings (Industrial Electronics Conference), IEEE Computer Society, 2007. p. 2152–2157.
20. Caner, C., Engin, M., and Engin, E.Z., *The Programmable ECG Simulator*. Journal of Medical Systems, 2008. **32**(4): p. 355–359.
 21. Karatas, F., Koyuncu, I., Alçın, M., and Tuna, M., *Design of FPGA-based ECG Signal Using VHDL*, 1st International Hazar Scientific Research Congress, IKSAD Publishing, Baku, Azerbaijan, 2020. p. 114–127.
 22. John, A.D., and Fleisher, L.A., *Electrocardiography: The ECG*. Anesthesiology Clinics of North America, 2006. **24**(4): p. 697–715.
 23. Alemzadeh-Ansari, M.J., Editor(s): Maleki, M., Alizadehasl, A., Haghjoo, M., *Chapter 3 Electrocardiography*, Practical Cardiology, 2018. p. 17-60.
 24. Wagner, G., *Chapter 6-Basic Electrocardiography*, Editor(s): Saksena, S., Camm, A.J., Boyden, P.A., Dorian, P., Goldschlager, N., *Electrophysiological Disorders of the Heart*, Churchill Livingstone, 2005. p. 95-128.
 25. SkillStat. *Free ECG Simulator*. [cited 2021 12 February]; Available from: <https://www.skillstat.com/tools/ecg-simulator/>.
 26. Tlelo-Cuautle, E., Rangel-Magdaleno, J., de la Fraga, L. G., Tlelo-Cuautle, E., Rangel-Magdaleno, J. de J., and De la Fraga, L. G., *Introduction to Field-Programmable Gate Arrays., Engineering Applications of FPGAs*, Springer International Publishing, 2016. p. 1–32.
 27. Alcin, M., Tuna, M., Erdogmuş, P., and Koyuncu, I., *FPGA-based Dual Core TRNG Design Using Ring and Runge-Kutta-Butcher based on Chaotic Oscillator*. Chaos Theory and Applications, 2021. **3**(1): p. 20–28.
 28. Moysis, L., Tutueva, A., Volos, C., and Butusov, D., *A Chaos Based Pseudo-Random Bit Generator Using Multiple Digits Comparison*. Chaos Theory and Applications, 2020. **2**(2): p. 58–68.
 29. Alçın, M., Pehlivan, İ., and Koyuncu, İ., *Hardware Design and Implementation of a Novel ANN-Based Chaotic Generator in FPGA*. Optik - International Journal for Light and Electron Optics, 2016. **127**(13): p. 5500–5505.
 30. Karataş, F., Koyuncu, İ., Tuna, M., and Alçın, M., *Bulanık Mantık Üyelik Fonksiyonlarının Fpga Üzerinde Gerçeklenmesi*. Bilgisayar Bilimleri ve Teknolojileri Dergisi, 2020. **1**(1): p. 1-9.
 31. Akgul, A., Calgan, H., Koyuncu, I., Pehlivan, I., and Istanbulu, A., *Chaos-Based Engineering Applications with a 3D Chaotic System without Equilibrium Points*. Nonlinear Dynamics, 2015. **84**(2): p. 481–495.
 32. Akgül, A., Arslan, C., Arıcıoğlu, B., *Design of an Interface for Random Number Generators based on Integer and Fractional Order Chaotic Systems*. Chaos Theory and Applications, 2019. **1**(1): p. 1–18.
 33. Pan, J., Luan, F., Gao, Y., and Wei, Y., *FPGA-Based Implementation of Stochastic Configuration Network for Robotic Grasping Recognition*. IEEE Access, 2020. **8**: p. 139966–139973.
 34. Fu, H., Osborne, W., Clapp, R. G., Mencer, O., and Luk, W., *Accelerating Seismic Computations Using Customized Number Representations on FPGAs*. Eurasip Journal on Embedded Systems, 2009. **382983**: p. 1-13.
 35. Koyuncu, I., Cetin, O., Katircioglu, F., and Tuna, M., *Edge Dedection Application with FPGA Based Sobel Operator*, 23rd Signal Processing and Communications Applications Conference (SIU), IEEE, Malatya, Turkey, 2015. p. 1829–1832.
 36. Taşdemir, M.F., Koyuncu, I., Coşgun, E., and Katircioglu, F., *Real-Time Fast Corner Detection Algorithm Based Image Processing Application on FPGA*, International Asian Congress on Contemporary Sciences-III, IKSAD Publishing, Konya, Türkiye, 2020. p. 1–6.
 37. Arshad, Shaukat, S., Ali, A., Eleyan, A., Shah, S., and Ahmad, J., *Chaos Theory and its Application: An Essential Framework for Image Encryption*. Chaos Theory and Applications, 2020. **2**(1): p. 17–22.
 38. Chowdhury, S.R., Chakrabarti, D., and Saha, H., *FPGA Realization of a Smart Processing System for Clinical Diagnostic Applications Using Pipelined Datapath Architectures*. Microprocessors and Microsystems, 2008. **32**(2): p. 107–120.
 39. Tuncer, T., Avaroglu, E., Türk, M., and Ozer, A.B., *Implementation of non-periodic sampling true random number generator on FPGA*. Informacije Midem, 2015. **44**(4): p. 296–302.
 40. Alinx Electronics Technology, *ZYNQ FPGA Development Board AX7020 User Manual*. [cited 2021 9 February]; Available from: <http://www.alinx.com/en/>.