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The Effect of Interface States and Series Resistance on Current-Voltage Characteristics in (MIS) Schottky Diodes

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Keywords
MIS Schottky Diode; Series Resistance; Ideality Factor; Interface States; Nitride Passivation

Abstract

The current-voltage (I-V) characteristics of metal-insulator-semiconductor (MIS) Al/Si_3N_4/p-Si Schottky barrier diodes (SBDs) were measured at room temperature. Al/Si_3N_4/p-Si structure has been fabricated by the electrochemical anodization method. The surface of p-type Si was passivated by nitridation process. Effects series resistance R_s , interfacial layer and interface states density (N_{ss}) on I-V characteristics were investigated. Al/Si_3N_4/p-Si (MIS) Schottky barrier diodes showed that rectifying behavior with an ideality factor value of 6.17 and barrier height value of 0.714 eV obeys a metal-interfacial layer – semiconductor (MIS) structure rather than an ideal Schottky diode due to the existence of Si_3N_4 at the Al/p-Si interfacial layer. The values of series resistance (R_s) were determined using Cheung's method. In addition, interface states density (N_{ss}) as a function of (E_{ss}-E_v) was extracted from the bias I-V measurements with and without taking into account the series resistance. The I-V characteristics confirmed that the distribution of N_{ss} , R_s and interfacial insulator layer are important parameters that influence the electrical characteristics of MIS Schottky diodes.

(MYY) Schottky Diyotlarda Akım-Voltaj Karakteristikleri Üzerine Seri Direnç ve Arayüzey Durumlarının Etkisi

Anahtar kelimeler
MYY Schottky diyot; Seri direnç; İdealite faktörü; Arayüzey durumları; Nitrit pasivasyonu

Özet

Metal-Yalıtkan-Yarıiletken (MYY) Al/Si_3N_4/p-Si Schottky engel diyotlarının akım-voltaj (I-V) karakteristikleri oda sıcaklığında ölçüldü. Al/Si_3N_4/p-Si yapılar elektrokimyasal anodizasyon metodu ile üretilmiştir. p tipi silisyumun yüzeyi nitridasyon işlemiyle pasive edildi. Akım-Voltaj karakteristikleri üzerine arayüzey durum yoğunluğu (N_{ss}), arayüzey tabakası ve seri direncin etkileri incelendi. Al/Si_3N_4/p-Si (MIS) Schottky engel diyotlar, Al/p-Si arayüzey tabakasındaki Si_3N_4 varlığı yüzünden ideal Schottky diyotlar yerine, idealite faktör değerinin 6.17 ve engel yüksekliği değerinin 0.714 eV olmasıyla doğrultucu davranış göstermesi, (MIS) metal- arayüzey tabakası- yarıiletken yapısına uyar. Seri direncin (R_s) değerleri Cheung' in metodu kullanılarak tanımlandı. Buna ilave olarak, (E_{ss}-E_v) nin bir fonksiyonu olarak, arayüzey durumlarının yoğunluğu (N_{ss}), seri direncin hesaba katıldığı ve katılmadığı I-V ölçümlerinden elde edildi. I-V karakteristikleri; N_{ss} dağılımı , R_s ve arayüzey yalıtkan tabakanın, MIS Schottky diyotların elektriksel karakteristiklerini etkileyen önemli parametreler olduğunu doğrulanmıştır.

1. Introduction

The existence of an insulator later (such as SiO_2 , Si_3N_4 , SnO_2) between a metal and semiconductor converts the MS structure into a MIS type structure. The interfacial insulator layer of metal-insulator-semiconductor (MIS) diodes plays an important role in the electrical characteristics of these structures and in the micro electronic devices. These type devices have important application in a wide variety of the optoelectronic, bipolar integrated circuits and high frequency applications. There are currently a vast number of experimental studies on diode characteristics parameters such as Schottky barrier heights (SBHs), ideality factor n, series resistance R_s and surface states N_{ss} in a great variety of MS and MIS type SBDs (Sze,1981;Cowley and Sze,1965; Card and Rhoderick,1971; Singh, et. al.1990; Cova and Singh,1990; Karataş, et.al.2003; Hudait,2001; Zhu, et.al.1999;Akkal,et.al.1988;Altındal,et.al.2003;Zeyrek, et.al. 2006;Taşcıoğlu,et.al.2014).

The characterization of a SBD with an interface layer does not obey the ideal Schottky theory. Especially understanding Schottky barrier formation between metal and semiconductor interface on a fundamental basis still remains a challenging problem. Also, Schottky barrier height, and ideality factor are the fundamental parameters of the MS or MIS structures and strongly effected devices performance.

The performance and reliability of these devices especially is depend on the formation of insulator layer between metal and semiconductor interface, the density of interface states distribution between semiconductor and insulator layer, series resistance and an inhomogeneous Schottky barrier contact. The first studies on the interfacial insulator layer, between metal and semiconductor, in Schottky diodes were made by Cowley and Sze (Cowley and Sze,1965) who obtained their estimations from an analysis of the Schottky barrier heights with different metallization as a function metal work function. Card and Rhoderick (Card and Rhoderick,1971) estimated the interface state density located at the oxide silicon interface and examined effects of the interface states on the ideality factor of the forward bias I-V characteristics.Some studies (Card and Rhoderick,1971; Singh, et. al.1990; Cova and Singh,1990; Akkal, et.al. 1988; Altındal,et.al.2003) inspected the effects of presence of an interfacial oxide layer and the interface states on the behaviour of Schottky diodes and extracted the density distribution of interface states in the semiconductor band gap from the forward bias I-V characteristics.

The formation of a direct insulator layer on Si by traditional ways of oxidation or deposition cannot completely passivate the active dangling bonds at the semiconductor surface. Recently, nitridation of silicon films receives much attention because silicon nitride film can suppress both of the leak current in insulating gate materials and interface reaction with metal oxide (Lee,et.al.2000). Thus, various non-traditional approaches for surface passivation such as ultra-thin sulphide, selenide layer or nitride formation have been a subject of increasing interest in recent years (Yüzer,et.al.2000). Also, the effect of nitride treatment is considered to be associated with passivation of the dangling bonds with nitride atoms and suppression of surface oxidation of Si. However, it has been reported that the passivated surface of Si was quickly degraded when it was exposed to air ambient.

In our previous work, we studied the temperature dependency of the main diode parameters forward bias current-voltage-temperature (I-V-T) characteristics of the Al/Si_3N_4/p-Si Schottky barrier diode at low temperatures (Zeyrek, et.al. 2006). In this work, we studied the effects of interface states and series resistance on current-voltage (I-V) characteristics of (MIS) Al/Si_3N_4/p-Si Schottky diode. Also, we studied to check the consistency of Cheung's approach only for room teemperature.

In this study, non-aqueous ammonium nitride ($(NH_4)_2(NH_2)_x$) electrolyte was employed for the first time to growth a nitride layer on the Si surface as a new method for nitride passivation. The purpose of this paper is to present the results of a systematic investigation of the effect N_{ss} and R_s on the I-V Characteristics of Al/Si_3N_4/p-Si (MIS) Schottky diode. In addition, this paper is purposed to form wide band gap Si_3N_4 insulator layer at Al/p-Si interface for the calculation of the interface states density with and without taking into account the series resistance R_s to see whether this interfacial layer has a passivation effect on I-V electrical characteristics and Al/Si_3N_4/p-Si (MIS)Schottky diode has a rectification behavior or not.

2. Experimental Procedure

$Al/Si_3N_4/p\text{-}Si$ (MIS) Schottky barrier diodes were fabricated on 2 inch diameter float zone (100) p-type (boron doped) single crystal silicon (Si) wafers having thickness 280 µm with 0.8 Ω cm resistivity. The sample was ultrasonically cleaned in trichloroethylene and ethanol, etched by CP4 (HNO_3 : HF : $COOHC_2H_5$: H_2O =3:1:2:2 weight ratio) solution 30 s. rinsed by propylene glycol and blown dry with nitrogen gas. Ohmic contacts of the electrodes were formed by evaporating Al in high vacuum ($P=10^{-6}$ Pa) and subsequently annealing them for a few minutes at 450 ^{o}C. After making of electrical contact, the walls and under side of the Si wafers were insulated with the high-quality wax.

The nitridation set-up, using in the study is the electrochemical anodization cell which consists of a p-Si anode and Pt as cathode. An agitation of the electrolyte is achieved by magnetic stirrer. Electrolyte used in the experiment was obtained by sequentially mixing of propylene glycol with ammonia (NH_3) and hydrazine (NH_2-NH_2) at 21:3:1 weight ratio, respectively. Preceding each cleaning step, the wafer was rinsed thoroughly in de-ionized water of resistivity of 18 MΩ-cm.

Immediately, the substrate was immersed in electrolytical cell. Anodic nitridation was performed using a constant current source at different current densities, under N_2 flow, in light and at room temperature (293 K). The potential difference between the electrodes normalised to calomel electrode was measured with an x-t recorder. The anodization was stopped, when the cell voltage reached about the 18 V. After the sample were immediately rinsed in propyl alcohol and blown dry nitrogen and left in a desiccator. The Schottky contacts were formed by evaporating of Al dots with diameter of about 1.0 mm and 2500 Å thick in high vacuum ($P=10^{-6}$ Pa). The metal thickness layer and the deposition rates were monitored with the help of quartz crystal thickness monitor. In this way, metal-interfacial insulator layer-semiconductor ($Al/Si_3N_4/p\text{-}Si$) Schottky barrier diodes were fabricated on p-type Si wafer. The interfacial insulator layer thickness (Si_3N_4) was estimated to be about 52 Å from measurement of the insulator capacitance in the strong accumulation.

The current-voltage (I–V) measurements were performed by the use of a Keithley 220 programmable constant current source, a Keithley 614 electrometer. All measurements were carried out with the help of a microcomputer through an IEEE 488 ac/dc converter card at room temperature.

3. Results and Discussions

The current through a Schottky barrier diode (SBD) at a forward bias V, according to thermionic emission (TE) theory, is given by (Sze,1981)

$$I = I_o \exp\left(\frac{q(V-IR_s)}{nkT}\right)\left[1-\exp\left(-\frac{q(V-IR_s)}{kT}\right)\right] \quad (1)$$

where I_0 is the reverse saturation current derived from the straight-line intercept of lnI at zero bias and is given by

$$I_o = AA^*T^2\exp\left(-\frac{q\Phi_{Bo}}{kT}\right) \quad (2)$$

where q is the electronic charge, A^* is the effective Richardson constant and equals to 32 A cm^{-2} K^{-2} for p-type Si, A is the effective diode area, k is the Boltzmann constant, T is the absolute temperature, Φ_{Bo} is the zero bias barrier height and n is the ideality factor. The ideality factor is calculated from the slop of the linear region of the forward bias ln(I)-V plot and can be written as from Eq.(1)

$$n = \frac{q}{kT}\left(\frac{d(V-IR_s)}{d(\ln I)}\right) \quad (3)$$

The zero-bias barrier height Φ_{B0} is determined from the extrapolated I_0 and is given by the relation:

$$\Phi_{b0} = \frac{kT}{q}\ln\left[\frac{AA^{*}T^{2}}{I_0}\right] \qquad (4)$$

Fig.1 shows a typical forward bias semi-log lnI-V characteristics of Al/Si_3N_4/p-Si (100) Schottky diode at room temperatures. Usually, the forward bias I-V characteristics are linear on a semilogarithmic scale at low forward bias voltages but deviate considerable from linearity due to the effect of series resistance R_s , the interfacial layer and interface states when the applied voltage is sufficiently large (Türüt, et. al. 1992; Çakar, et.al. 2002; Cova, et.al. 1998). The series resistance is significant in the downward curvature (non-linear region) of the forward bias I-V characteristics, but the other parameters (n and Φ_{Bo}) are significant in both the linear and non-linear regions of the I-V characteristics.

The experimental values of n and Φ_{Bo} were determined from Eq.(3) and (4), respectively, shown is Table 1. As shown in Table 1, the experimental values of Φ_{Bo} and n for the Al/Si_3N_4/p-Si (100) Schottky diodes range from 0.714 eV and 6.17 at room temperature, respectively.

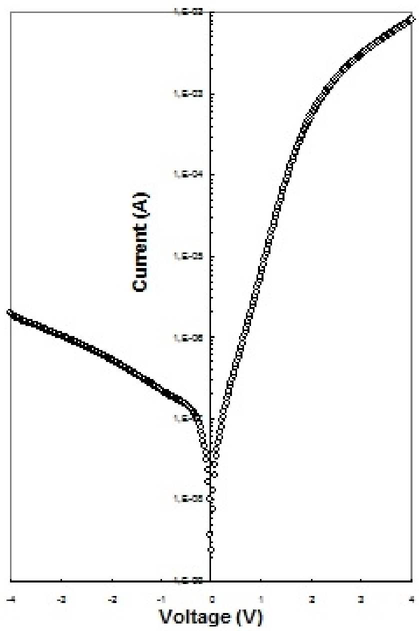

Figure 1. The forward and reverse-bias I-V characteristics of the MIS Schottky diode at room temperature.

This value of ideality factor obtained from the forward bias I-V plot is greater than unity, indicating the presence of a thin interface insulator layer between the Al layer and p-Si semiconductor. Such behavior of ideality factor has been attributed to particular distribution of interface states and insulator layer between metal and semiconductor (Card and Rhoderick,1971; Altındal,et.al.2003).

The density distribution curves of the interface states N_{ss} in equilibrium with the semiconductor can be determined from the forward bias I-V characteristics at room temperature. The effective barrier height Φ_e is assumed to be bias-dependent due to the presence of an interfacial insulator layer and interface states located between interfacial layer and semiconductor interface and it is given by

$$\frac{d\Phi_e}{dV} = \beta = \left(1 - \frac{1}{n(V)}\right) \qquad (5)$$

Voltage-dependent ideality factor n(V) can be written from Eq.(1) as

$$n(V) = \frac{q}{kT}\left(\frac{d(V - IR_s)}{d(\ln I / I_0)}\right) \qquad (6)$$

where β is the voltage coefficient of the effective barrier height Φ_e and is given by (Singh,1990; Cova and Singh,1990; Altındal, et.al. 2003).

$$\Phi_e = \Phi_{Bo} + \beta(V - IR_s) = \Phi_{Bo} + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \qquad (7)$$

For metal-insulator-semiconductor (MIS) diode having interface states N_{ss} in equilibrium with semiconductor, the ideality factor n becomes greater unity and is given by

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \quad (8a)$$

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_s}{W_D}\right] \quad (8b)$$

where δ is the thickness of interfacial insulator layer, W_D is the width of the space charge region, ε_i and ε_s are the permittivity of the interfacial insulator layer and the semiconductor, respectively. The thickness δ can be obtained for MIS Schottky diode from sufficiently high frequency (f≥500 kHz) C-V measurements using the equation $C_i=\varepsilon_i\varepsilon_s A/\delta$, where C_i is the capacitance of the interfacial insulator layer.

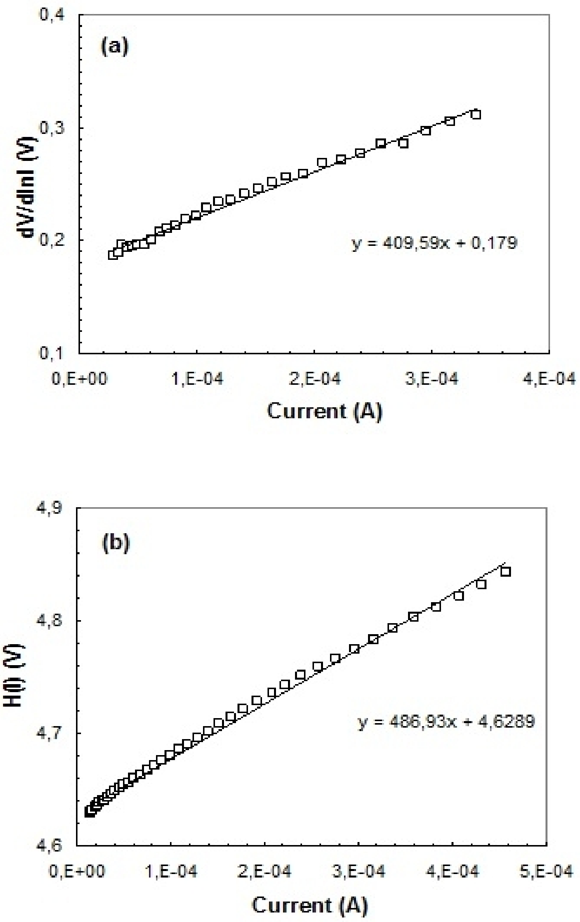

Figure 2. (a) Experimental dV/dlnI vs. I and (b) H(I) vs. I plots for the MIS Schottky diode.

Furthermore, in p-type semiconductors, the energy of N_{ss} with respect to the top of valance band at the surface of the semiconductor is given by

$$E_{ss} - E_v = q(\Phi_e - V) \quad (9)$$

Usually, the forward bias current voltage (I-V) characteristics are linear in the semilogarithmic at low voltages but deviate considerably from linearity due to the effect of parameters such as R_s and N_{ss} when the applied voltage is sufficiently large. The values series resistance R_s, ideality factor n and zero-bias barrier height Φ_{Bo} were carried out using another method developed by Cheung and Cheung (Cheung and Cheung,1986). The Cheung's functions given as

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right) \quad (10)$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \quad (11)$$

$$H(I) = IR_s + n\Phi_{B0} \quad (12)$$

where Φ_{B0} the barrier height obtained from data of downward curvature region in the forward bias I-V characteristics. The term IR_s is the voltage drop across series resistance of diode. Voltage V_d= V- IR_s across the diode can be expressed in terms of total voltage drop V acros the series combination of the diode and the series resistance . In Fig. 2a and 2b , experimental dV/d(lnI) vs. I and H(I) vs. I plots are presented at room temperature. Eq. (10) should give a straight line for the data of downward curvature region in the forward bias I-V characteristics. Thus, a plot of dV/d(lnI) versus I will give R_s as the slope and nkT/q as the y-axis intercept.

Also, Fig.2b obtained from Eq. 12 shows the plot of H(I) versus I and gives a straight line with the y-axis intersept equal to $n\Phi_{B0}$. The slope of this plot also provides the second determination of R_s, which can be used to check the consistency of Cheung's approach.

Thus, the slope and y-axis intercept of a plot of dV/dlnI vs. I will give R_s with the value of 410 Ω and n value of 6.91, respectively. Using the n value of 6.91, the slope and y-axis intercept of a plot of H(I) vs. I will give R_s with the value of 487 Ω and barrier height value 0.66 eV, respectively.

The values of series resistance calculated from Eq.10 and Eq.12 are presented in Table 1. It can be seen obviously that the value of R_s obtained from H(I)–I plots is in close agreement with the value obtained from dV/d(lnI)–I plot. This case shows the consistency of the Cheung's approach (Akkal, et.al. 1988; Kar, et.al. 1982; Feteha,et.al.2002; Beji,et.al.2006; Tataroğlu and Altındal,2008; Ebeoğlu,2008).

The energy distribution profiles of the interface states N_{ss} was obtained from the forward bias I-V characteristics by taking into account the bias dependence of the effective barrier height Φ_e with and without series resistance R_s . The value of N_{ss} were calculated from Eq.(8b), by taking the values of voltage-dependent n(V) , ε_s=11.8 ε_o , ε_i=7.5ε_o and δ=52 Å. These values of N_{ss} were converted to a function of E_{ss}-E_v using Eq.(9).

Fig. 3 shows the density of interface states N_{ss} distribution profiles as a function E_{ss}-E_v at room temperature. The exponential increase of the interface states density from midgap towards the top of the valance band is very apparent (Card and Rhoderick,1971; Tataroğlu and Altındal,2008; Hackam and Harrop,1972; Arshak,et.al.2003 ; Hudait and Krupanidhi,2002).

As can be seen in Fig.3, the magnitude of the N_{ss} with and without the R_s at 0.58-E_v (eV) has changed in the range from 4.19x10^{13} to 4.64x10^{13} eV^{-1}cm^{-2}, respectively. The N_{ss} values obtained taking into account the series resistance are lower than those obtained without taking into account the series resistance. The N_{ss} obtained without taking into account the series resistance has exponential increased from 0.58-E_v (eV) to 0.66-E_v (eV) in the interval. The N_{ss} obtained taking into account the series resistance has remained nearly constant with value of 4.19x10^{13} eV^{-1}cm^{-2} in the same interval even though interface state density has little increased. This is attributed to the nitridation of the p type Si surface due to the Si_3N_4 insulator layer formed by method of electrochemical anodization (Ebeoğlu,2008). The above explanations clearly show that the R_s value should be taken into account in determining the interface state density distributions profiles (Karataş, et.al.2005; Karataş and Altındal,2005; Karataş and Türüt,2006; Dökme,2007).

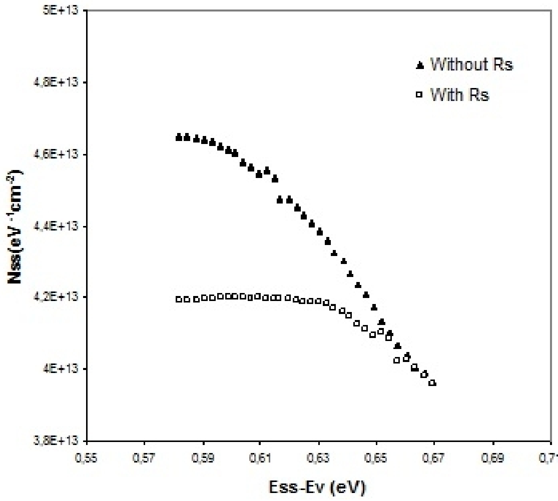

Figure 3. The density of interface states (Nss) distribution profiles as a function Ess-Ev obtained from the forward bias I-V characteristics.

Table1.Various parameters determined from I-V characteristics of (MIS) Al/Si_3N_4/p-Si Schottky diode.

n (I-V)	n dV/d(lnI)	Φ_{Bo} (I-V)(eV)	Φ_{Bo} (H(I))(eV)	R_s dV/d(lnI)(Ω)	R_s (H(I))(Ω)
6.17	6.91	0.714	0.66	410	487

4. Conclusion

In this work, the effect of interface states and series resistance on current-voltage characteristics in (MIS) Al/Si_3N_4/p-Si Schottky barrier diode has been investigated. The non-ideal forward bias I-V behavior observed in the (MIS) $Al/Si_3N_4/p\text{-}Si$ Schottky barrier diode was attributed to a change in the metal-semiconductor barrier height due to the insulator layer, interface states and series resistance. The applied bias voltage drops partially across the interface layer causing the forward current to drop, thus this case has resulted in strong deviation from ideal I-V characteristics. The values of ideality factor and barrier height have been calculated as 6.17 and 0.714 eV , respectively, from forward bias I-V measurements. The n value obtained from I-V characteristics are higher than unity, and that is attributed to the presence of interfacial insulator layer between the metal and semiconductor. The ideality factor n, barrier height Φ_{B0} , series resistance R_s , and interface states density N_{ss} for this diode have been calculated by the forward bias I-V measurements. The downward curvature at sufficiently large voltages is caused by the effect of series resistance R_s , apart from the presence of the interface states, which are in equilibrium with the semiconductor. The value of the R_s has been calculated from high voltage region of the structure by using Cheung functions. It is seen that there is a good agreement between the values of the series resistance obtained from two Cheung plots. As can be seen from the results, series resistance value should be taken into account in determining the interfacial state density distribution curves.

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