Research Article GU J Sci, Part A, 10(2): 206-221 (2023) 10.54287/gujsa.1303347

Gazi University
Journal of Science
PART A: ENGINEERING AND INNOVATION
http://dergipark.org.tr/gujsa

A Control Scheme for a Quasi-Z Source Three-Phase Inverter

Zafer ORTATEPE[1*] Sadık ÖZDEMİR[2]

[1]*Pamukkale University, Department of Automotive Engineering, Denizli, Türkiye*
[2]*Pamukkale University, Department of Mechatronics Engineering, Denizli, Türkiye*

Keywords

DC-AC Inverter
Modulation Scheme
Quasi-z Source Inverter

Abstract

This paper presents a novel control scheme for a three-phase quasi-z source inverter (qZSI) using a capacitor voltage and input current-based sinusoidal pulse width modulation (SPWM) technique. The proposed scheme combines the advantages of both qZSI and SPWM techniques to achieve improved performance. The SPWM technique utilizes a sinusoidal modulation signal, which is compared with a high-frequency triangular carrier wave and two shoot-through (ST) references to determine the switching states for the three-phase qZSI. The positive and negative ST references are obtained from the capacitor voltages and input current, allowing for control of the DC bus voltage and ST states of the inverter. Additionally, the proposed control scheme generates the three-phase modulation signal through decoupling control in the dq reference frame. The detailed analysis of the control scheme includes its operating principle, transient state, steady-state responses, and the effects of parameter variations. Simulation studies are conducted using MATLAB/Simulink to assess the performance of the three-phase qZSI under the proposed control scheme. The simulation results demonstrate the effectiveness of the control scheme in terms of output voltage quality, DC bus voltage control, and robustness against reference variations. Overall, the proposed capacitor voltage and input current-based SPWM control scheme for the three-phase qZSI shows promising performance improvements and robustness, as confirmed through comprehensive simulation studies.

Cite

Ortatepe, Z., & Özdemir, S. (2023). A Control Scheme for a Quasi-Z Source Three-Phase Inverter. *GU J Sci, Part A*, *10*(2), 206-221. doi:10.54287/gujsa.1303347

Author ID (ORCID Number)

0000-0001-7771-1677 Zafer ORTATEPE
0000-0001-7676-7484 Sadık ÖZDEMİR

Article Process

Submission Date 27.05.2023
Revision Date 19.06.2023
Accepted Date 21.06.2023
Published Date 23.06.2023

1. INTRODUCTION

Three-phase voltage source inverters (VSIs) have found extensive application in the field of power electronics. However, despite their widespread use, they are not without limitations. Specifically, VSIs can generate harmonic distortions in the output waveform and have constraints in achieving higher output voltages beyond the input DC voltage.

Z-source inverter (ZSI) has been proposed as a solution to overcome the disadvantages associated with conventional VSIs (Peng, 2002; 2003; Peng et al., 2003). The ZSI is designed with a unique impedance network in its DC input circuit. Some of the advantages of ZSIs include the ability to provide voltage boost capability, which is useful in applications that require higher output voltage levels than the input source voltage can provide. Additionally, ZSIs offer inherent short-circuit protection (Parla & Özdemir, 2022). However, ZSIs also have some limitations, including discontinuous input current.

To overcome these drawbacks, a new qZSI topology is proposed as a modified version of ZSI to achieve similar functionalities with lower-rated passive components (Anderson & Peng, 2008a; 2008b; Cao & Peng, 2009). The qZSI topology features a continuous input current and enables operation at a wide range of input

*Corresponding Author, e-mail: zortatepe@pau.edu.tr

voltages, making it suitable for diverse applications (Hong & Cha, 2021; Li et al., 2022; Elmorshedy et al., 2023). Additionally, the topology has two operation modes: non-shoot-through (NST) state and shoot-through (ST) state (Paikray et al., 2022). The diode network and LC connected to qZSI change the operation of the topology to allow an ST state. In the ST state, the inverter voltage shoots through the impedance source network like a short circuit, allowing the qZSI to act as a voltage buck/boost without the need for an additional DC/DC converter (Liu et al., 2019; Poorali & Adib, 2020). However, the ST state is undesirable, as it can result in high current flow, and potentially cause damage to the inverter (Sun et al., 2013; Padmavathi & Natarajan, 2020).

Proper control and modulation techniques have been employed to ensure the safe and reliable operation of the qZSI (Endiz & Akkaya, 2022). Various PWM modulation methods have been studied to achieve less device stress, less switching/commutation, and simple applicability over a wide modulation range in three-phase qZSI applications (Devaraj et al., 2019; Mohammadi et al., 2020; Nguyen & Choi, 2021). Although many modulation techniques have been studied in the literature, SPWM is the primary modulation technique employed in three-phase qZSI circuits. SPWM modulation has been applied to the qZSI with four basic ST methods, including maximum constant boost control, maximum boost control, simple boost control, and third-harmonic injection. Each method has its own advantages and disadvantages.

In this paper, the ST state references are identified from the capacitor voltages and input current to control the DC bus and ST states of qZSI. Besides, three-phase reference modulation signals are generated using the decoupling control method in a dq reference frame. A high-frequency triangular carrier wave, three-phase sinusoidal modulation signals, and two positive and negative ST references obtained from the input capacitor voltages and input current of the qZS network are used to determine ST and NST switching states of the qZSI.

Following the introduction, the paper is organized as follows: Section 2 presents the three-phase qZSI mathematical model. Then, Section 3 introduces the decoupling control in a dq reference frame and SPWM control methods, followed by a discussion of the results. Finally, the article concludes with a conclusion and recommendations section.

2. MATHEMATICAL MODEL OF THREE-PHASE QZSI

Figure 1 illustrates the equivalent circuit of a three-phase qZSI. The qZS network comprises two capacitors (C_1, C_2), two inductors (L_1, L_2), and one diode (D). V_{in} represents the DC input voltage of the qZS network, while V_{PN} represents the connection point between the qZS network and the conventional three-phase VSI and serves as the DC input voltage of the conventional three-phase inverter. For the mathematical analysis conducted in this paper, the inductances and capacitors of the qZS network are assumed to be equivalent as indicated by Equations (1) and (2).

$$L_1 = L_2 = L \tag{1}$$

$$C_1 = C_2 = C \tag{2}$$

2.1. Non-Shoot-Through State

Figure 2 illustrates the equivalent circuit of the active (non-shoot-through) state of the three-phase qZSI. During the NST state operation, the three-phase VSI is treated as a current source. In this state, the energy stored during the ST state is transferred to the load. The instantaneous load current (i_{load}) is equal to the inverter input current (i_{inv}) as indicated by Equation (3).

$$i_{inv} = i_{load} \tag{3}$$

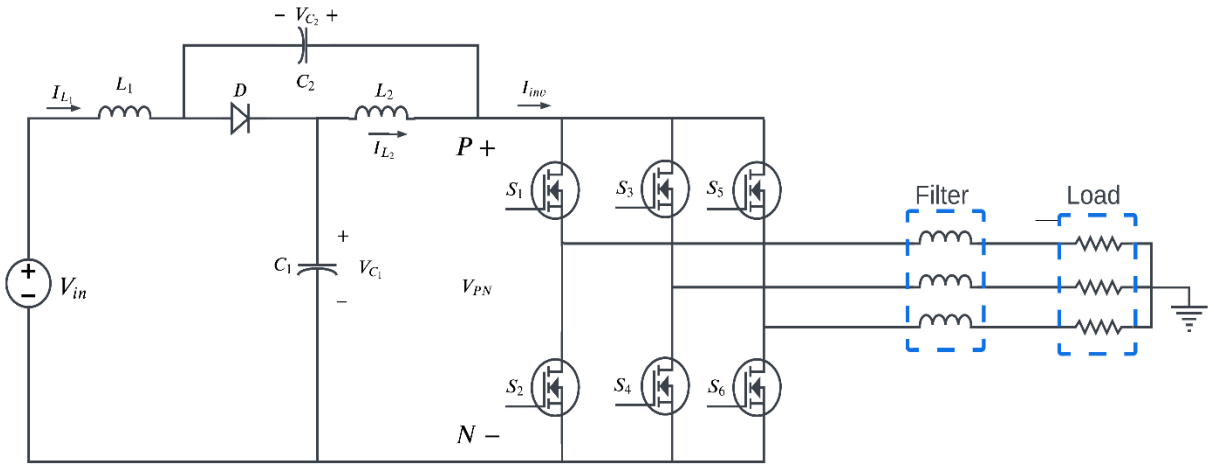


Figure 1. *Three-phase qZSI equivalent circuit*

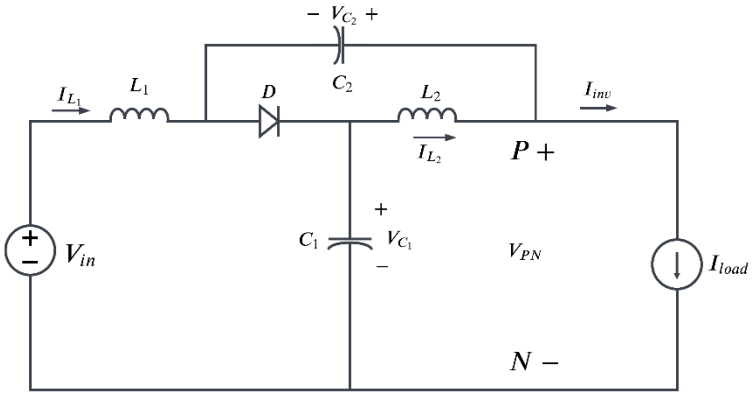


Figure 2. *NST state operation of the qZSI*

The inductance current (i_{L_1}) can be derived from the equivalent circuit for the NST state as shown in Equation (4):

$$L\frac{di_{L1}}{dt} = V_{in} - v_{C1} \tag{4}$$

The C_1 capacitor voltage (v_{C_1}) can also be derived using the equivalent circuit depicted in Figure 2. The equation that describes the derivation of C_1 capacitor voltage is given by Equation (5).

$$C\frac{dv_{C1}}{dt} = i_{L1} - i_{inv} \tag{5}$$

In Equation (6), the variables ($S_a,\ S_b,\ S_c$) represent integer values that can take the numbers 0 and 1. A value of 0 indicates that the corresponding switch is in the off state, while a value of 1 indicates that the switch is in the on state. On the other hand, ($i_a,\ i_b,\ i_c$) represent the three-phase load currents.

$$i_{inv} = S_a i_a + S_b i_b + S_c i_c \tag{6}$$

2.2. Null State

Figure 3 presents the equivalent circuit of the null state of a three-phase qZSI. In the null state operation, all the switches of the VSI are in the off state, meaning that no current flows through the VSI.

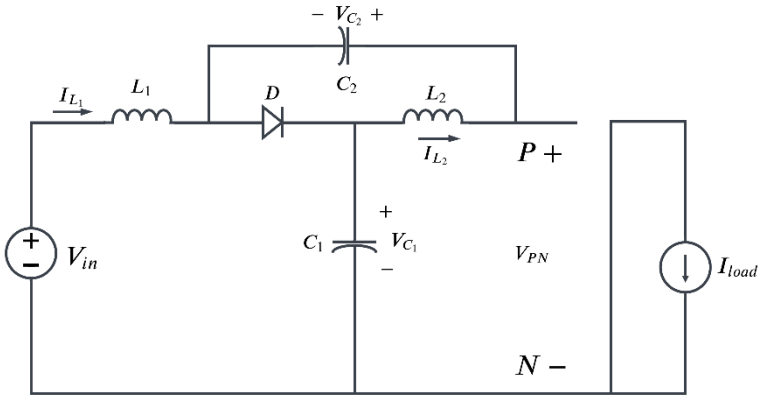


Figure 3. *Null state operation of the qZSI*

From Figure 3, the expression for the inductance current (i_{L_1}) of the L_1 inductance and the equation for the capacitor voltage (v_{C_1}) of the C_1 capacitor can be derived. These equations are represented as Equations (7) and (8), respectively.

$$L\frac{di_{L1}}{dt} = V_{in} - v_{C1} \tag{7}$$

$$C\frac{dv_{C1}}{dt} = i_{L1} \tag{8}$$

2.3. Shoot-Through State

Figure 4 illustrates the equivalent circuit of the ST state in a three-phase qZSI. Unlike a conventional VSI, during the ST state, the lower and upper switches of each phase in the three-phase qZSI are short-circuited. This configuration allows the qZS network to store energy from the DC bus, leading to voltage boosting. The voltage boosted during the ST operation can then be transferred to the load during the NST state. It's important to note that during the ST state, the diode of the qZS network is off. This is because the polarity of the capacitors C_1 and C_2 blocks the diode D from conducting.

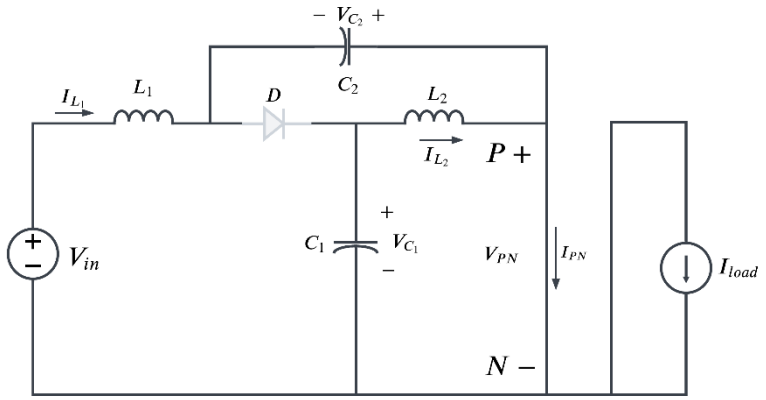


Figure 4. *ST state operation of the qZSI*

The L_1 inductance current (i_{L_1}) and the capacitor C_1 voltage (v_{C_1}) equations can be obtained from Figure. 4 as given in Equations (9) and (10), respectively.

$$L\frac{di_{L1}}{dt} = V_{in} + v_{C2} \tag{9}$$

$$C\frac{dv_{C1}}{dt} = -i_{L2} \tag{10}$$

According to Kirchoff's voltage law, the relationship between the input voltage and capacitor voltages is expressed in Equation (11), and as shown in Figure 4, inductance currents are equal to Equation (12).

$$v_{C1} - v_{C2} = v_{in} \tag{11}$$

$$i_{L1} = i_{L2} \tag{12}$$

2.4. Decoupling Control in dq Reference Frame

Equations (13) to (15) provide the representation of the virtual three-phase output voltages. In the equations, V_{max} represents the maximum voltage and ω the angular frequency.

$$v_a = V_{max}sin(\omega t) \tag{13}$$

$$v_b = V_{max}sin(\omega t - 2\pi/3) \tag{14}$$

$$v_c = V_{max}sin(\omega t + 2\pi/3) \tag{15}$$

The equations giving the relationship between the three-phase load and inverter are shown in Equation (16). This equation is defined in (abc) stationary reference frame.

$$\begin{bmatrix} di_a \\ di_b \\ di_c \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{L}\begin{bmatrix} u_a - v_a \\ u_b - v_b \\ u_c - v_c \end{bmatrix} \tag{16}$$

By performing the park transformation, the equation given above (16) in the stationary reference frame can be converted to the synchronously rotating reference frame as given in Equation (17). In this equation, i_d and i_q are d-axis and q-axis output currents, v_d and v_q are d-axis and q-axis load voltages and u_d and u_q are d-axis and q-axis inverter voltages, respectively.

$$\begin{bmatrix} \frac{di_d}{dt} \\ \frac{di_q}{dt} \end{bmatrix} = \frac{1}{L}\begin{bmatrix} -R & \omega L \\ -\omega L & -R \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} - \frac{1}{L}\begin{bmatrix} v_d \\ v_q \end{bmatrix} + \frac{1}{L}\begin{bmatrix} u_d \\ u_q \end{bmatrix} \tag{17}$$

Equations (18) and (19) give the decoupling dq-axis inverter voltages in the synchronously rotating reference frame. In these equations, inverter voltage is formulated as the sum of load voltage and other coupling parameters.

$$u_d = L\frac{di_d}{dt} + Ri_d - \omega Li_q + v_d \tag{18}$$

$$u_q = L\frac{di_q}{dt} + Ri_q - \omega Li_d + v_q \tag{19}$$

The reference and measured dq-axis load voltages are compared, and its PI controller output gives dq-axis reference currents as given in Equations (20) and (21). This reference dq-axis currents and the measured and transformed dq-axis output currents are compared with the PI controller to make the closed-loop controller stable in the decoupling control. Its formulation is given in Equations (22) and (23).

$$i_{d_{ref}} = \left(K_{p_1} + \frac{K_{i_1}}{s}\right)\left(V_{d_{ref}} - V_d\right) \tag{20}$$

$$i_{q_{ref}} = \left(K_{p_2} + \frac{K_{i_2}}{s}\right)\left(V_{q_{ref}} - V_q\right) \tag{21}$$

$$u_d = \left(K_{p_3} + \frac{K_{i_3}}{s}\right)\left(i_{dref} - i_d\right) - \omega Li_q + V_d \tag{22}$$

$$u_q = \left(K_{p_4} + \frac{K_{i_4}}{s}\right)\left(i_{dref} - i_q\right) - \omega Li_q + V_d \tag{23}$$

The decoupling control of three-phase qZSI is shown in Figure 5.

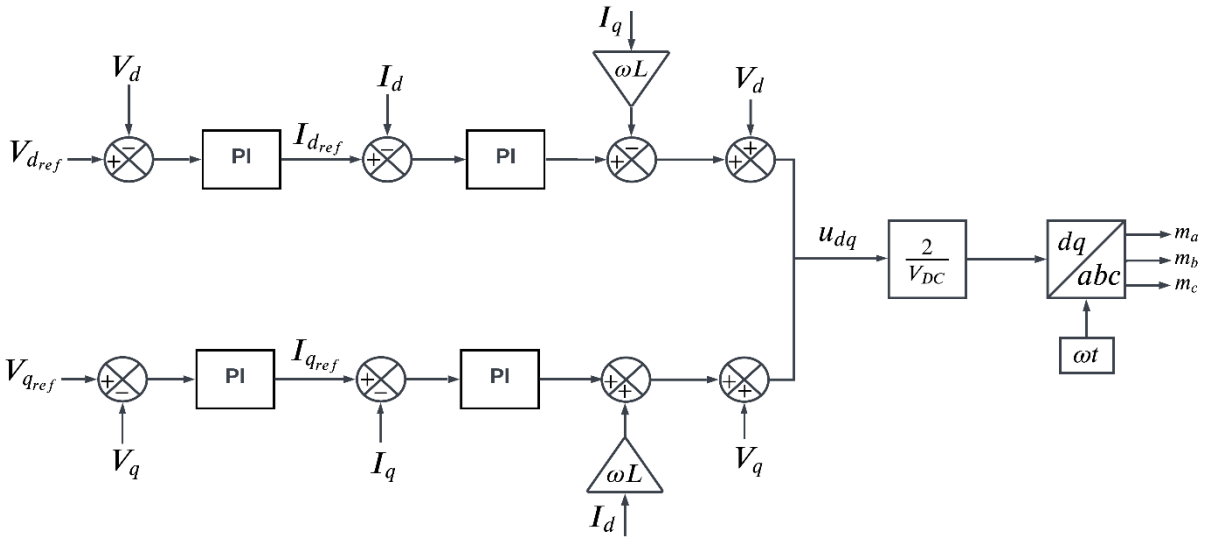


Figure 5. *Modulation control strategy in dq reference frame*

2.5. Sinusoidal PWM (SPWM) Control Strategy

The fundamental concept behind SPWM is to utilize a sine wave to modulate the duty cycle of a square wave. In SPWM, the output signal takes on a waveform resembling a sine wave, and its fundamental frequency matches the frequency of the modulating sine wave. A waveform with variable amplitude and frequency is produced when the square wave's duty cycle varies proportionally to the sine wave's amplitude. Simple boost control, maximum boost control, maximum constant boost control, and third-harmonic injection are the main SPWM modulation techniques (Sabeur et al., 2018; Zhao et al., 2019; Garcia-Vazquez et al., 2020; Xu et al., 2020).

In this paper, ST state references are identified from the capacitor voltages and input current to control DC bus voltage and ST states of qZSI. The positive and negative ST state (+D and -D) generation control block diagram is given in Figure 6. Reference ($V_{C_{ref}}$) and the sum of actual capacitor voltages ($V_{C_1} + V_{C_2}$) are compared, and its output gives reference input current as given in Equation (24). This reference and the measured input currents are compared in the PI controller to obtain the ST state of the qZSI as given in Equation (25).

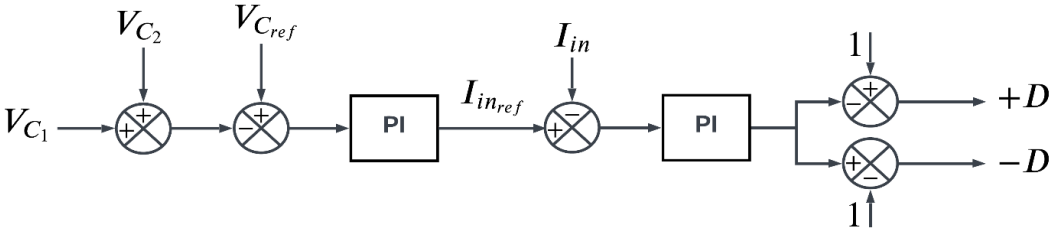


Figure 6. *Positive and negative ST state (+D and -D) generation control block diagram*

$$I_{in_{ref}} = \left(K_{p_5} + \frac{K_{i_5}}{s}\right)\left(V_{C_{ref}} - \left(V_{C_1} + V_{C_2}\right)\right) \tag{24}$$

$$1 - D = \left(K_{p_6} + \frac{K_{i_6}}{s}\right)\left(I_{in_{ref}} - I_{in}\right) \tag{25}$$

Figure 7 shows the generation of switching signals of a three-phase qZSI by decoupling control and ST state control methods. To generate the +D and -D references, the sum of capacitor voltages ($V_{C_1} + V_{C_2}$) of the qZS network is compared with reference capacitor voltage ($V_{C_{ref}}$). Error is employed to PI controlled to generate qZS network input current reference. +D and -D references are generated by adding ± 1 output obtained by comparing the measured input current with the PI controller respectively.

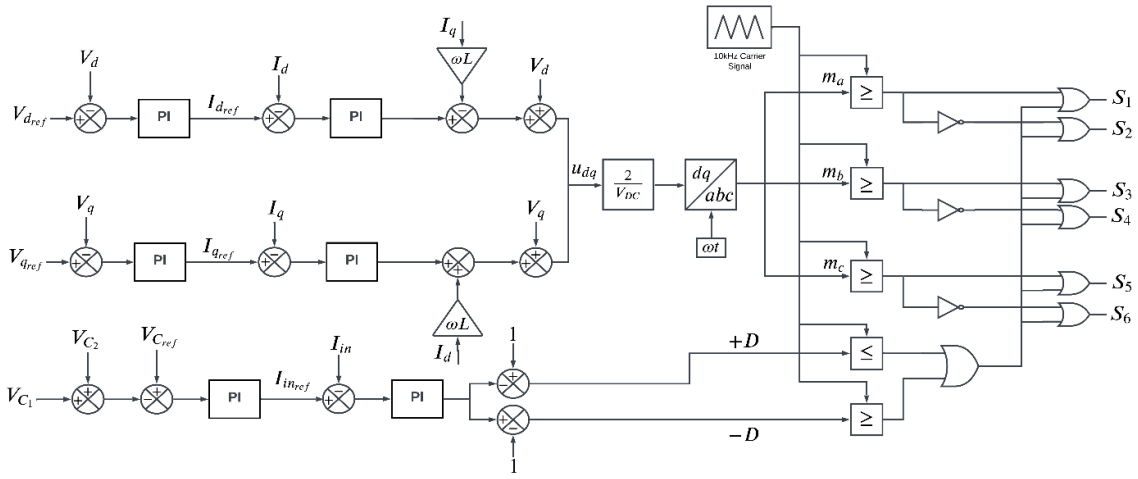


Figure 7. *Modulation and ST state control with SPWM controller*

The control layout of three-phase qZSI is given in Figure 8. Output voltages and currents measured at the load are converted to the synchronously rotating reference frame. The resulting dq-axis output currents are used to generate inverter reference voltages in the current controller. The generated reference inverter voltages and the measured output voltages converted to the dq axis are used to generate the reference dq axis output voltages using the decoupling control equations. The calculated dq-axis output reference voltages are transformed to a stationary abc-axis reference frame and (m_a, m_b, m_c) voltage references are obtained.

The sum of the capacitor voltages V_{C1} and V_{C2} of the qZS network is compared with the reference capacitor voltage. This reference capacitor voltage also equals the maximum DC bus voltage. Reference input current is generated by passing the error through PI control. The obtained input reference current is compared with the actual/measured input current and the difference is subjected to PI control. The PI controller output is used to have +D and -D references.

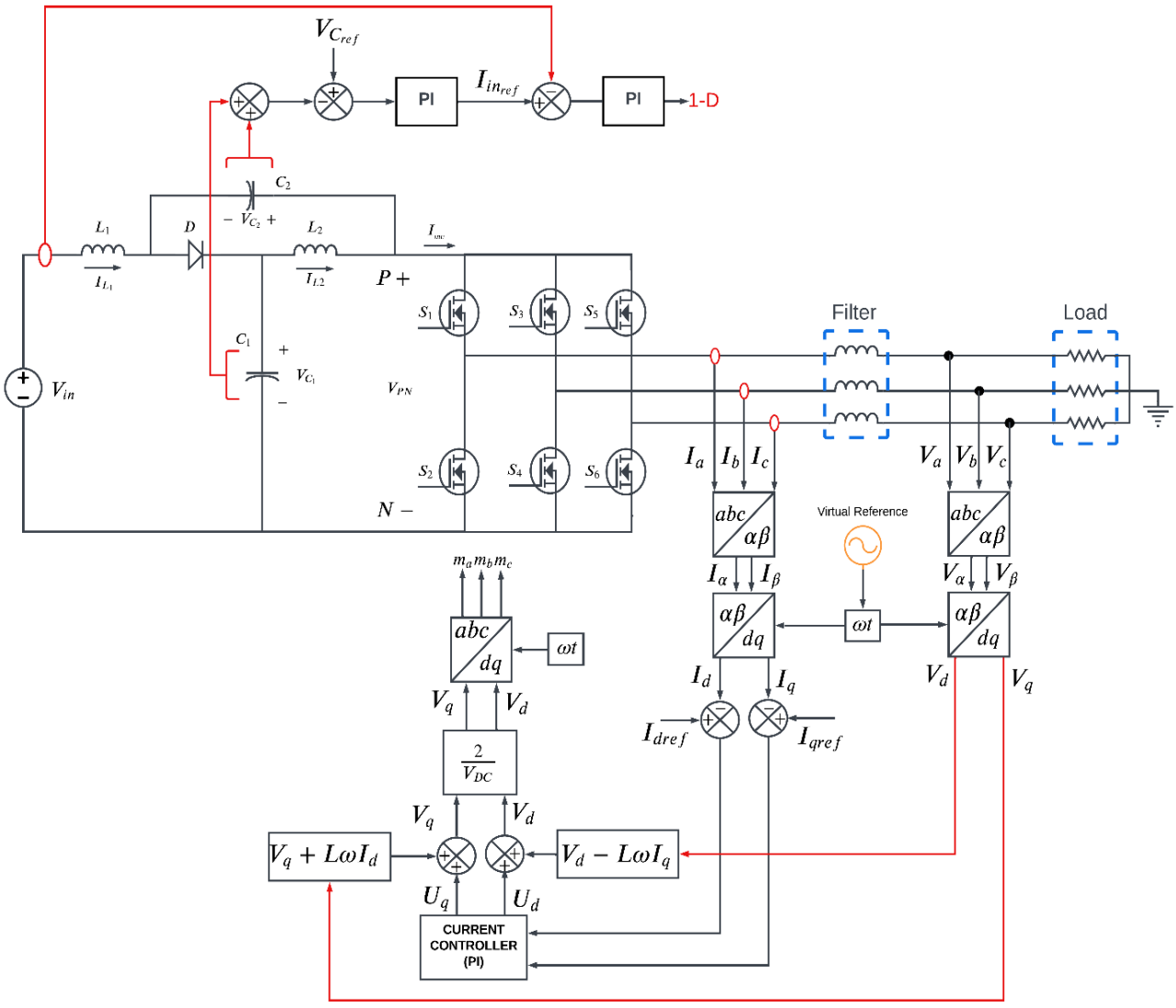


Figure 8. *The control layout of the three-phase qZSI*

3. SIMULATION RESULTS

Simulation studies have been performed with Matlab/Simulink program to evaluate the performance of three-phase qZSI. Moreover, the whole control scheme of the qZSI is designed in Matlab/Simulink. Therefore, the parameters used in the paper are presented in Table 1.

Table 1. *Simulation parameters are used in this paper.*

Parameters	Symbols	Values
Input voltage	V_{in}	100 [V_{dc}]
Output load	R_L	40 [Ω]
Filter inductance	L_f	10 [mH]
Switching frequency	f_s	10 [kHz]
DC bus voltage	V_{PN}	800 [V_{dc}]
qZSI Inductances	L_1,L_2	500 [µH]
qZSI Capacitors	C_1,C_2	300 [µF]

Also, the layout of the whole control system of qZSI is depicted in Figure 9. Decoupling control and ST state control scheme are given on the upper side, and three-phase qZSI is given on the lower side. DC bus voltage is determined as 800 V_{dc}. All inductance and capacitor values are selected as 500 µH and 300 µF, respectively. Besides, the switching frequency is selected as 10kHz. Finally, the output filter and resistive load parameters are determined as 10 mH and 40 Ω, respectively.

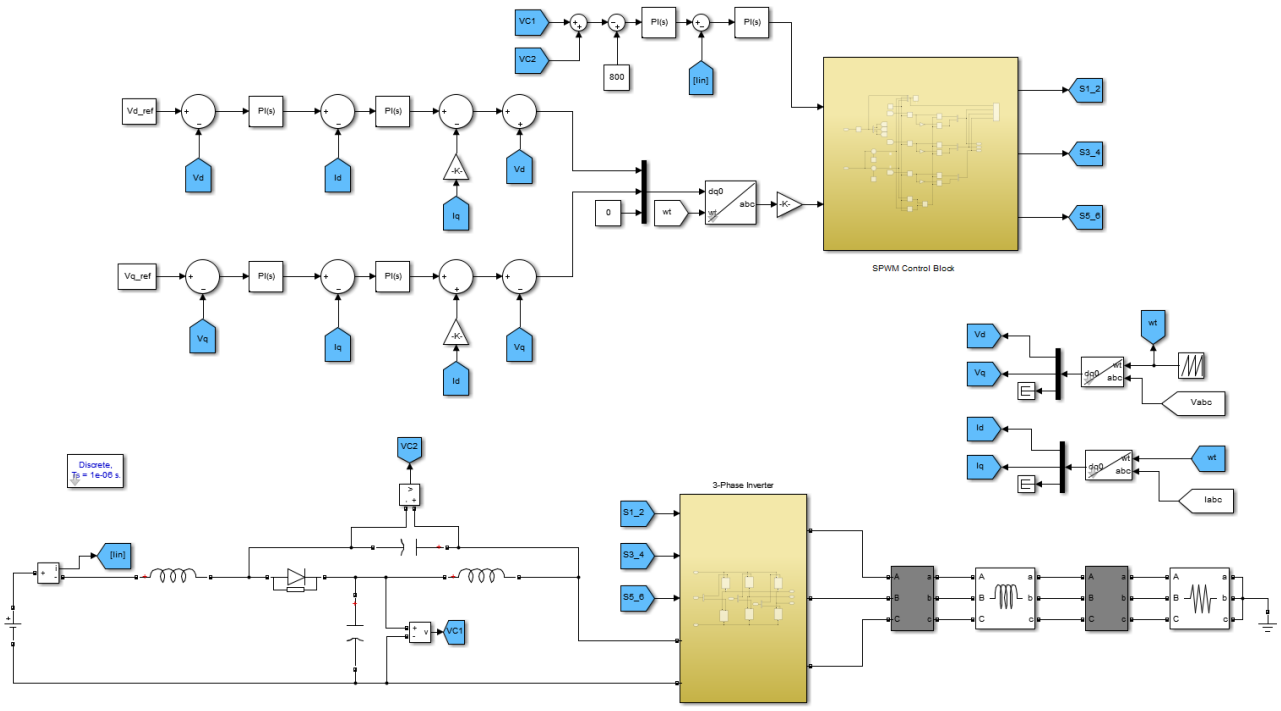


Figure 9. *The layout of the whole control system of the qZSI*

Besides, the six PI controller parameters used in the simulation are also shown in Table 2. PI_1 and PI_2 controllers are responsible for generating the $I_{d_{ref}}$ and $I_{q_{ref}}$, respectively. PI_3 and PI_4 controllers are responsible for generating the u_d and u_q, respectively. Finally, PI_5 and PI_6 controllers are responsible for generating the ST state as $1-D$.

Table 2. *PI parameters used in the qZSI controller.*

Parameters	Symbols	Values
PI_1	K_{P_1}, K_{I_1}	0.001, 0.2
PI_2	K_{P_2}, K_{I_2}	0.001, 0.2
PI_3	K_{P_3}, K_{I_3}	5, 5000
PI_4	K_{P_4}, K_{I_4}	5, 5000
PI_5	K_{P_5}, K_{I_5}	0.06, 5
PI_6	K_{P_6}, K_{I_6}	1.5, 0.01

The proposed control scheme and qZSI are analyzed in transient, steady state, and some parameter variations. Figure 10 depicts the steady-state capacitor and bus voltages of the SPWM-based three-phase qZSI. In typical operating conditions, the bus voltage is equal to the sum of V_{C_1} and V_{C_2}. However, when the system is in the ST state, the output voltage is zero. Furthermore, it can be deduced that the input voltage, V_{in_1}, is equal to the difference between V_{C_1} and V_{C_2}.

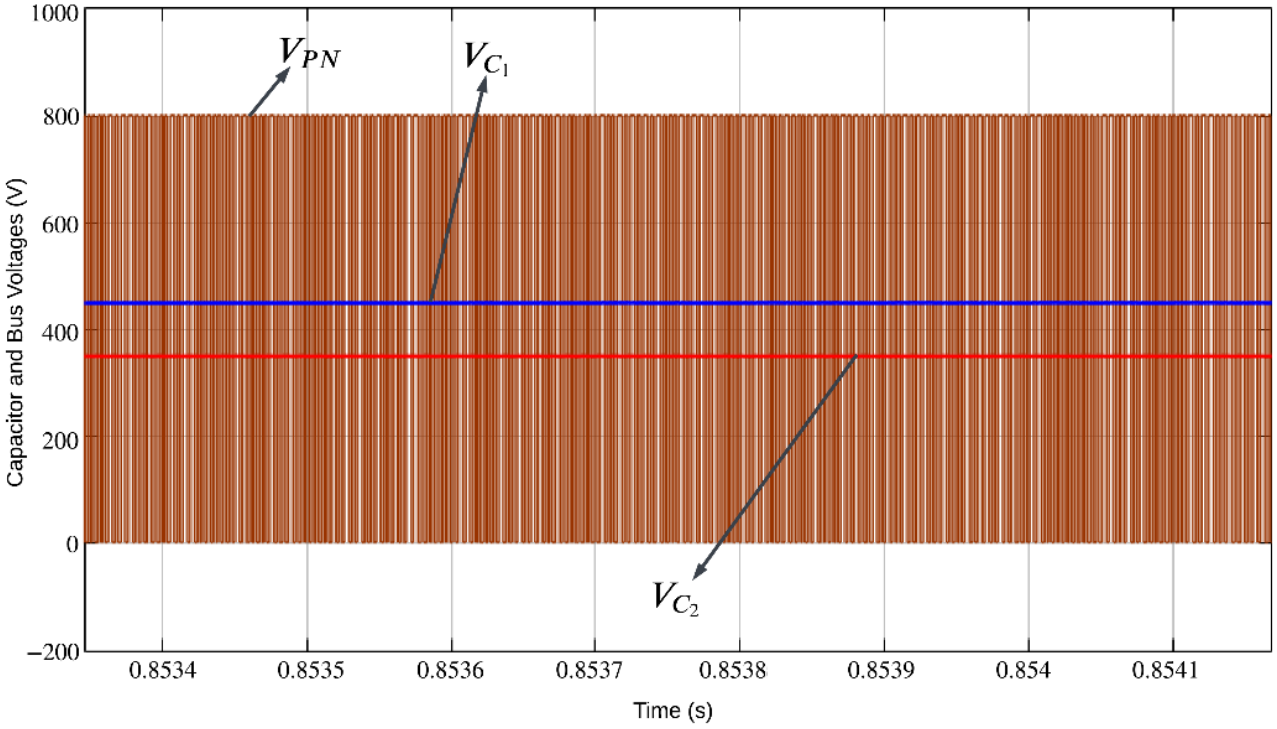


Figure 10. *Capacitor (V_{C_1},V_{C_2}) and bus voltage (V_{PN}) waveforms of the SPWM-based qZSI*

Transient state output voltage (V_d,V_q) and output current (I_d,I_q) waveforms of the SPWM-based three-phase qZSI in a dq reference frame are illustrated in Figure 11. To observe the transient response of the circuit, $V_{d_{ref}} = 311V$ and $V_{q_{ref}} = 0V$ are applied to the input as reference voltages and the output current $I_d \cong 4A$ and $I_q \cong -2.15A$ are obtained. It has been observed that all current and voltage values are set to a 2 % reference band at approximately 300 ms.

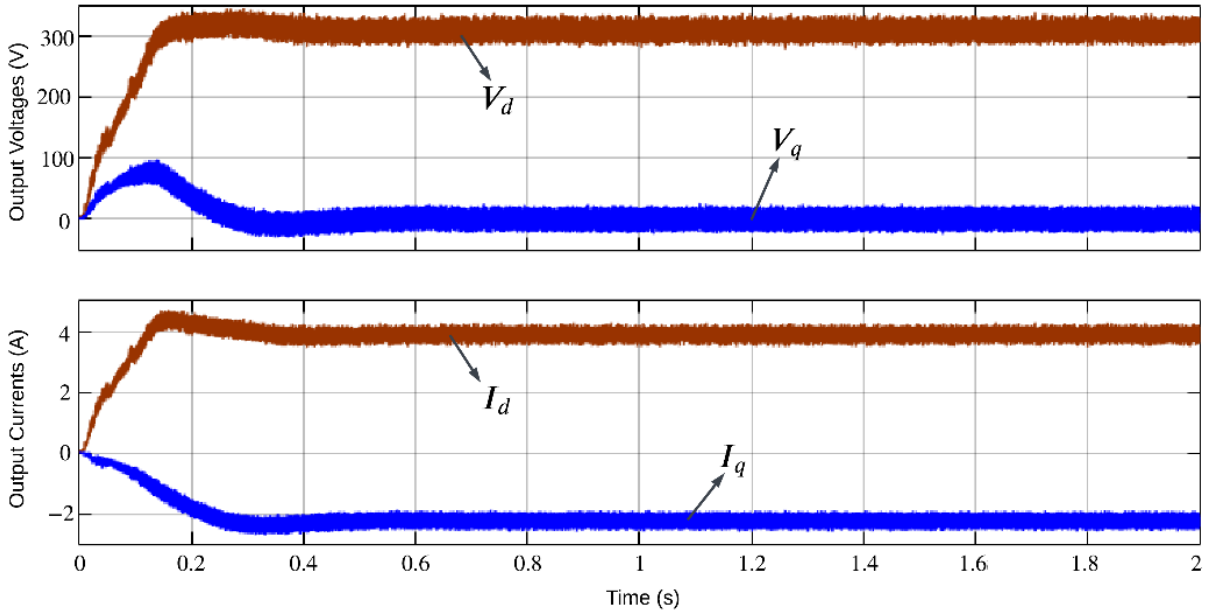


Figure 11. *Output voltage (V_d, V_q) and output current (I_d, I_q) waveforms of the SPWM-based qZSI in a dq reference frame.*

Steady-state phase-neutral output voltages (V_{an}, V_{bn}, V_{cn}) and filtered output current ($I_{o_a}, I_{o_b}, I_{o_c}$) waveforms of the SPWM-based three-phase qZSI are given in Figure 12, respectively. $V_{d_{ref}} = 311V$ and $V_{q_{ref}} = 0V$ are applied to the input as reference voltages to examine the steady response of the circuit and the maximum value of the balanced output current $I_{o_a} \cong I_{o_b} \cong I_{o_c} \cong 4.9A$ are obtained. The filtered output current has a sinusoidal form while the input voltage has three-level square waveform. Moreover, the THD value of the output current is measured as 3.9 % and it can be concluded that the THD value of the input current is acceptable limits for IEC61000-3-2.

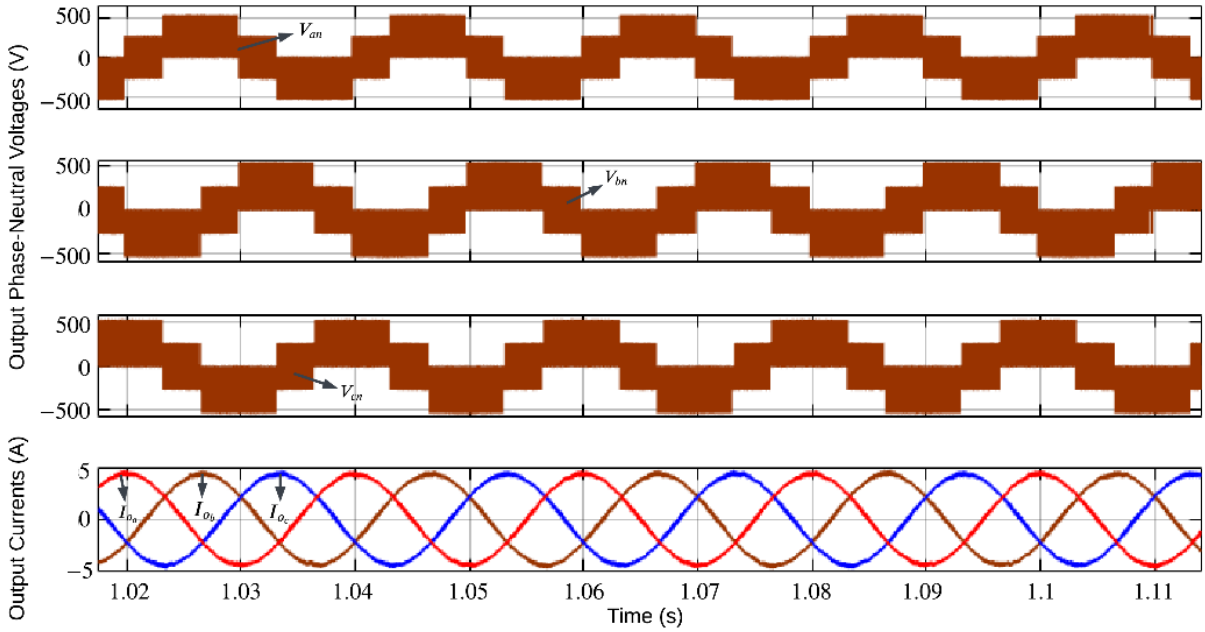


Figure 12. *Output phase-neutral voltages (V_{an}, V_{bn}, V_{cn}) and filtered output current ($I_{o_a}, I_{o_b}, I_{o_c}$) waveforms of the SPWM-based qZSI*

Steady-state filtered output phase-phase voltages (V_{ab}, V_{bc}, V_{ca}) and output current ($I_{o_a}, I_{o_b}, I_{o_c}$) waveforms of the SPWM-based three-phase qZSI are shown in Figure 13, respectively. It can be inferred that all filtered current and voltage waveforms of qZSI are sinusoidal in a steady state.

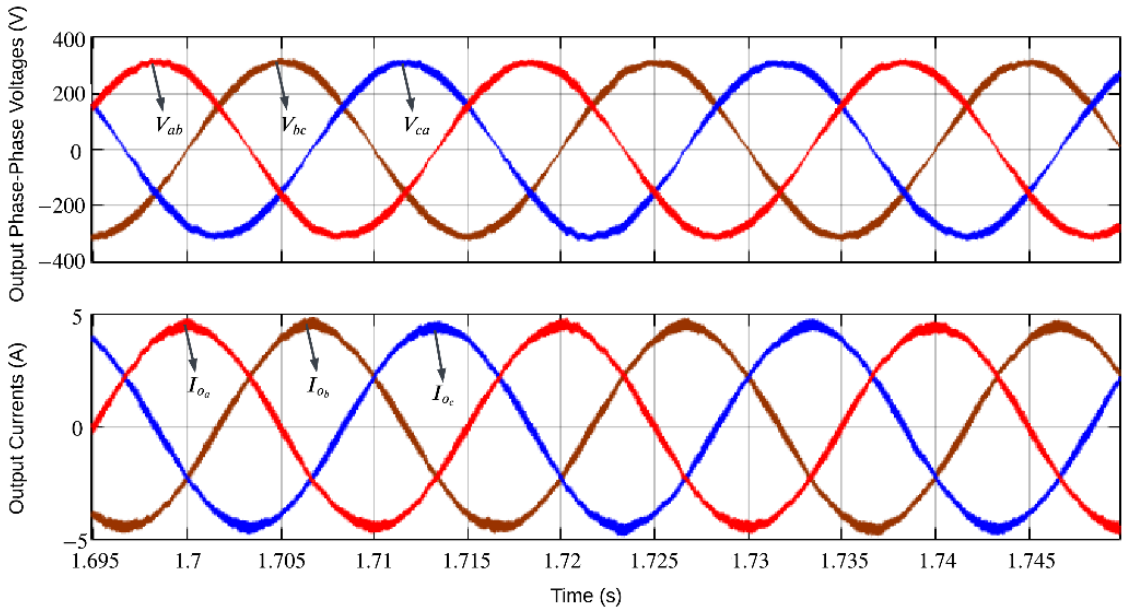


Figure 13. *Filtered output phase-phase voltages (V_{ab}, V_{bc}, V_{ca}) and output current ($I_{o_a}, I_{o_b}, I_{o_c}$) waveforms of the SPWM-based qZSI*

Step responses of the output voltage (V_d, V_q), output current (I_d, I_q), phase-phase output voltage (V_{ab}, V_{bc}, V_{ca}), and output current ($I_{o_a}, I_{o_b}, I_{o_c}$) waveforms of the SPWM-based three-phase qZSI are depicted in Figure 14, respectively. To study the step response of the circuit, $V_{d_{ref}} = 311V$ and $V_{q_{ref}} = 0V$ are applied to the input as reference voltages. After 0.7 seconds, $V_{d_{ref}} = 200V$ and $V_{q_{ref}} = 0V$ are applied as a reference, and after 1.4 seconds, $V_{d_{ref}} = 200V$ and $V_{q_{ref}} = -150V$ are applied, respectively. In all cases, the system settles to the 2 % reference band at a maximum of 200 ms.

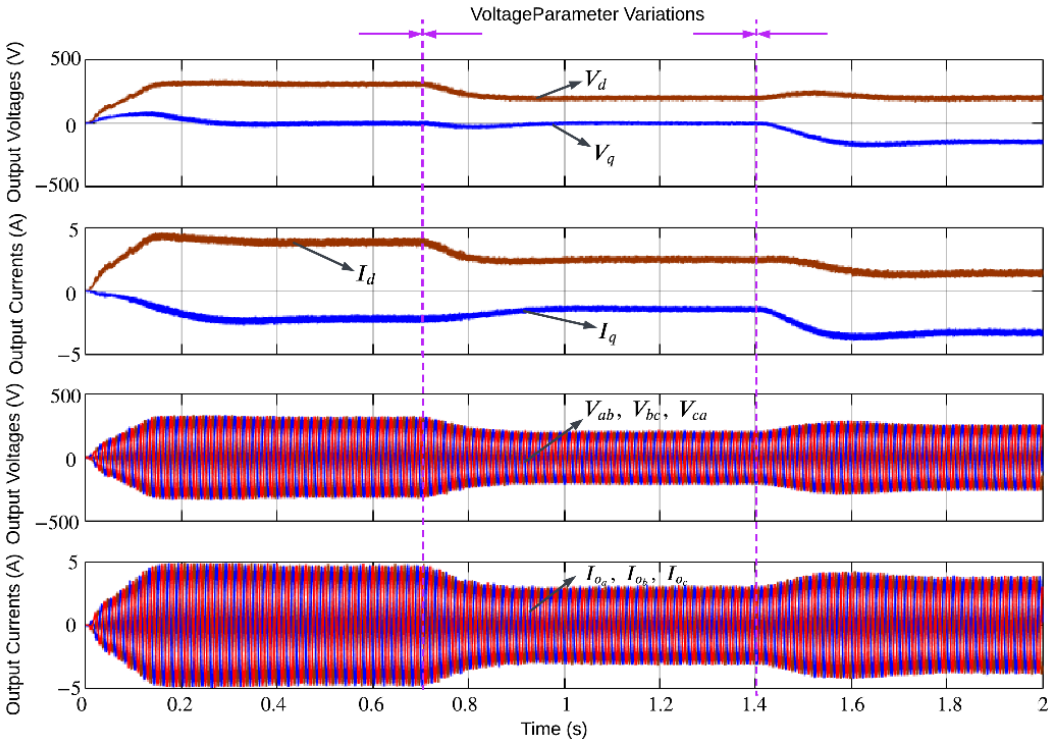


Figure 14. *Output voltage (V_d, V_q), output current (I_d, I_q), phase-phase output voltage (V_{ab}, V_{bc}, V_{ca}), and output current ($I_{o_a}, I_{o_b}, I_{o_c}$) waveforms of the SPWM-based qZSI*

Step responses of the capacitor voltages (V_{C_1}, V_{C_2}) and input current (I_{in}) waveforms of the SPWM-based three-phase qZSI are illustrated in Figure 15, respectively. To analyze the step response of the circuit, $V_{d_{ref}} = 311V$ and $V_{q_{ref}} = 0V$ are applied to the input as reference voltages. After 0.7 seconds, $V_{d_{ref}} = 200V$ and $V_{q_{ref}} = 0V$ are applied as a reference, and after 1.35 seconds, $V_{d_{ref}} = 200V$ and $V_{q_{ref}} = -150V$ are applied, respectively. In a transient state, maximum voltage ripples of the capacitor voltages V_{C_1} and V_{C_2} are obtained as 2 %. Moreover, it has been observed that the capacitor voltages do not change in the steady state even if the reference voltage variations and settle to the reference after a few hundred milliseconds.

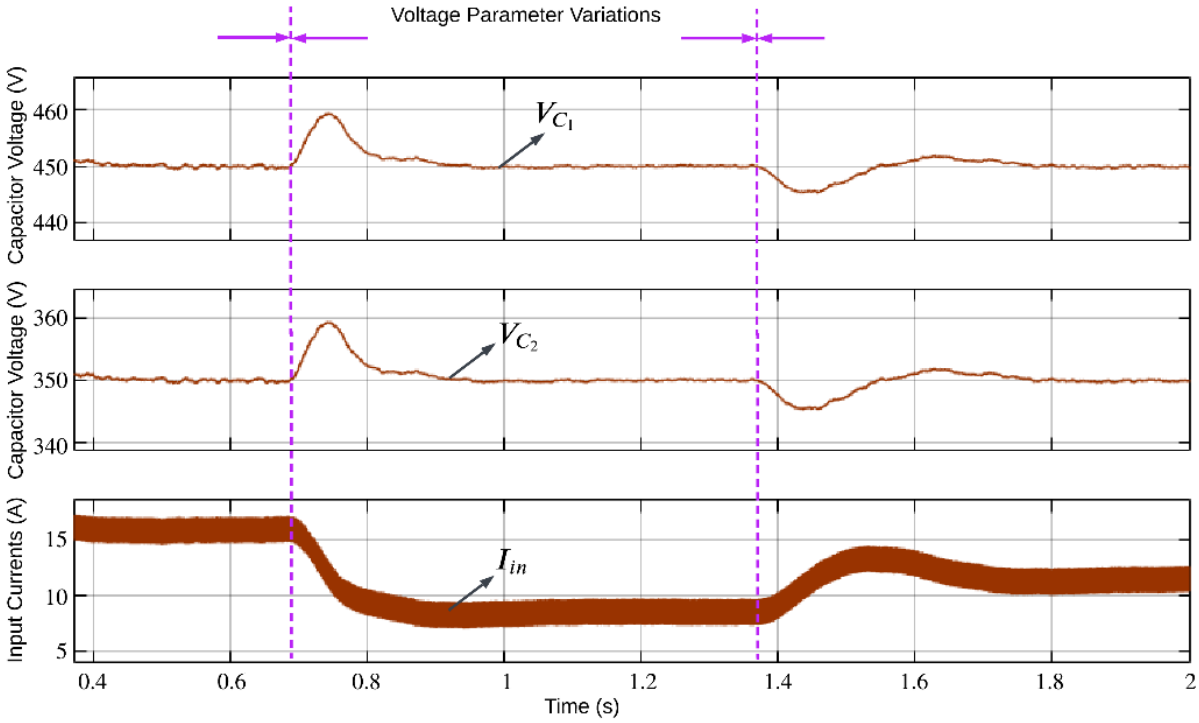


Figure 15. *Capacitor voltages (V_{C_1}, V_{C_2}) and input current (I_{in}) waveforms of the SPWM based qZSI*

Step responses of the output voltage (V_d, V_q), output current (I_d, I_q), phase-phase output voltage (V_{ab}, V_{bc}, V_{ca}), and output current ($I_{o_a}, I_{o_b}, I_{o_c}$) waveforms of the SPWM-based three-phase qZSI are depicted in Figure 16, respectively. To study the step response of the circuit, $I_{d_{ref}} = 3A$ and $I_{q_{ref}} = 0A$ are applied to the input as reference currents. After 0.7 seconds, $I_{d_{ref}} = 1A$ and $I_{q_{ref}} = 0A$ are applied as a reference, and after 1.35 seconds, $I_{d_{ref}} = 1A$ and $I_{q_{ref}} = -3A$ are applied, respectively. In all cases, the system settles to the 2 % reference band at a maximum of 100 ms. In this case, it can be deduced that the response of the system to the current reference is about two times faster than the response to the voltage reference.

Current harmonic limits of the SPWM based three-phase qZSI under full load and half load conditions are shown in Figure 17a and 17b, respectively. According to the figure, IEC61000-3-2 Class C harmonic limits are met for both conditions, and the THD value of the output current is measured as 3.9 % for the full load condition and 4.5 % for the half load condition.

Figure 18 shows the PF values for different load conditions for the SPWM-based three-phase qZSI output current. As can be seen from the figure that the power factor increases from half load to full load. Moreover, it can be deduced from the figure that the PF is about 99 % under all load conditions after half load.

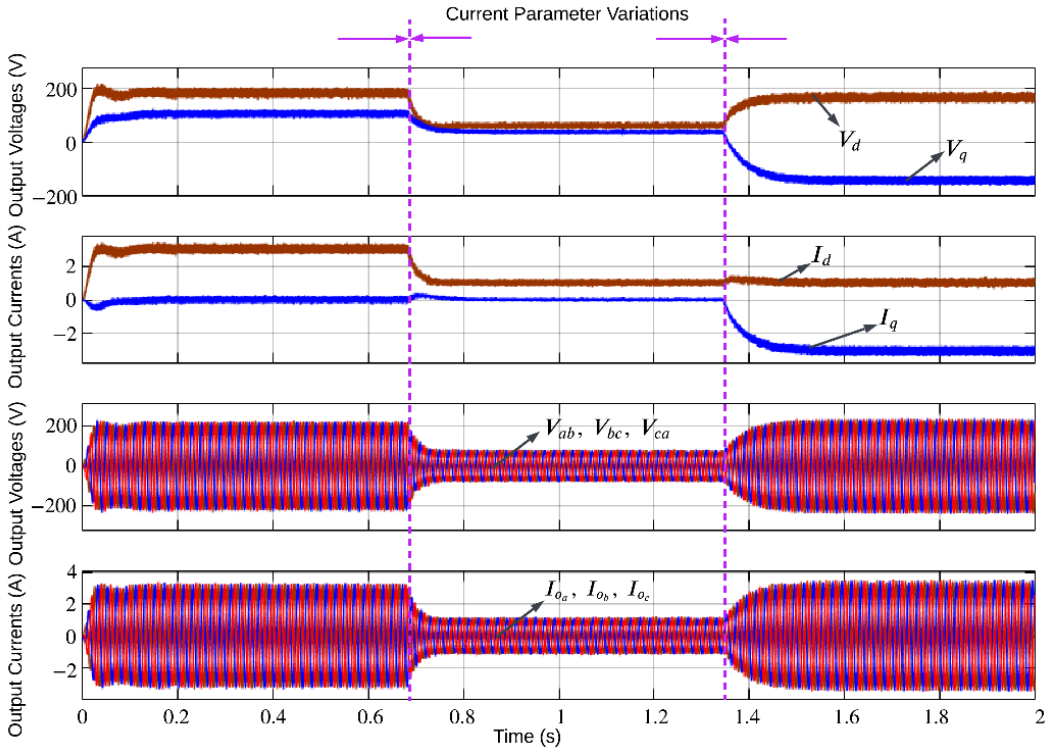
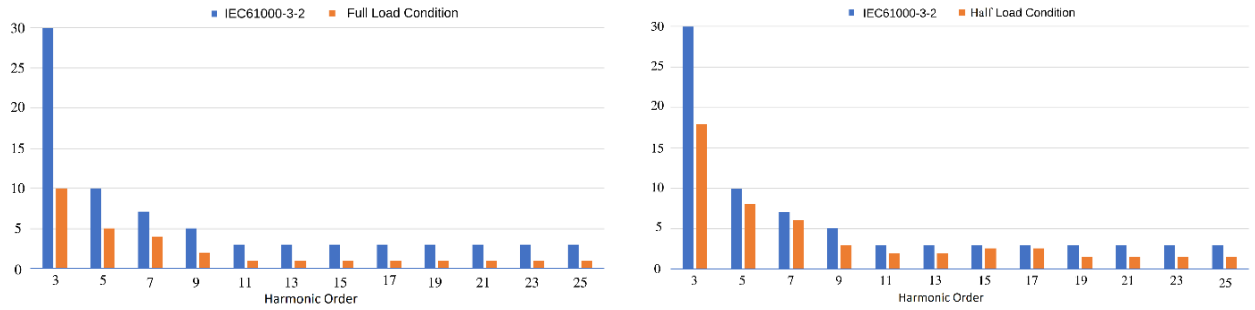


Figure 16. *Output voltage (V_d, V_q), output current (I_d, I_q), phase-phase output voltage (V_{ab}, V_{bc}, V_{ca}), and output current ($I_{o_a}, I_{o_b}, I_{o_c}$) waveforms of the SPWM-based qZSI*



(a) (b)

Figure 17. *Current harmonic limits of qZSI* ***a)*** *full load condition* ***b)*** *half load condition*

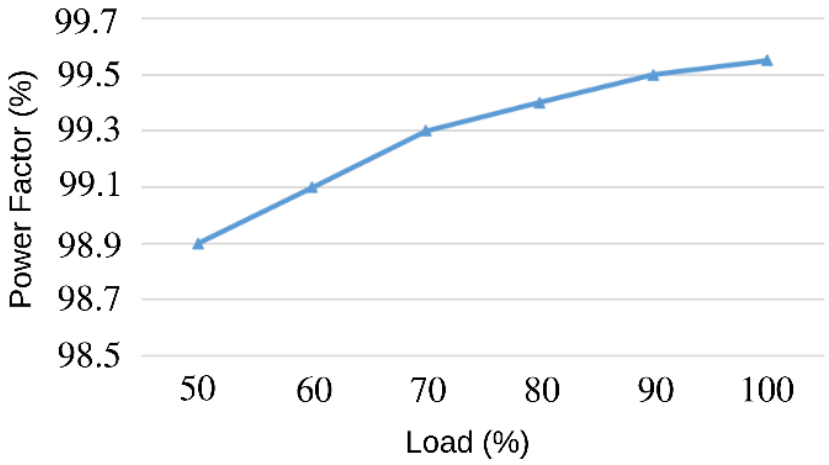


Figure 18. *Power factor (PF) measurement of the output current under different load conditions*

4. CONCLUSION

In this paper, a capacitor voltage and input current-based SPWM control scheme for a three-phase qZSI has been extensively tested and analyzed under various conditions. The circuit underwent thorough testing in transient, steady-state, and parameter change scenarios, and consistently exhibited excellent performance.

Furthermore, the inverter was subjected to separate tests for both current and voltage references, and it demonstrated precise tracking of all the references. This indicates that the circuit is capable of accurately controlling both the current and voltage, making it a reliable power source suitable for a wide range of applications.

The current THD value was consistently found to be below 5 % under different parameter and load change conditions. This outcome highlights the inverter's ability to generate high-quality output current while complying with the current harmonic limits specified by the IEC61000-3-2 Class C standard.

Overall, the proposed control scheme presents a promising solution for power conversion, as it effectively reduces harmonic distortion and enables accurate control of current and voltage. The scheme's performance has been thoroughly tested and analyzed, showcasing its potential for diverse applications.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

REFERENCES

Anderson, J., & Peng, F. Z. (2008a, October 5-9). A Class of Quasi-Z-Source Inverters. In: Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS), Edmonton, Canada. doi:10.1109/08IAS.2008.301

Anderson, J., & Peng, F. Z. (2008b, June 15-19). Four quasi-Z-Source inverters. In: Proceedings of the 39th IEEE Annual Power Electronics Specialists Conference (PESC), (pp. 2743-2749), Rhodes, Greece. doi:10.1109/PESC.2008.4592360

Cao, D., & Peng, F. Z. (2009, February 15-19). A family of Z-source and Quasi-Z-source DC-DC converters. In: Proceedings of the Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), (pp. 1097-1101), Washington, USA. doi:10.1109/APEC.2009.4802800

Devaraj, U., Ramalingam, S., & Sambasivam, D. (2019). Evaluation of Modulation Strategies for Single-Phase Quasi-Z-Source Inverter. *Journal of The Institution of Engineers (India): Series B*, *100*(4), 333-341. doi:10.1007/s40031-019-00378-z

Elmorshedy, M. F., Essawy, I. J. A., Rashad, E. M., Islam, M. R., & Dabour, S. M. (2023). A Grid-Connected PV System Based on Quasi-Z-source Inverter with Maximum Power Extraction. *IEEE Transactions on Industry Applications*, 1-11. doi:10.1109/TIA.2023.3275557

Endiz, M. S., Akkaya, R. (2022). Performance Analysis of Z-Source Inverter Control Techniques. *El-Cezerî Journal of Science and Engineering*, *9*(2), 625-633. doi:10.31202/ecjse.990144

Garcia-Vazquez, C. A., Sanchez-Sainz, H., Gonzalez-Rivera, E., Llorens-Iborra, F., & Fernandez-Ramirez, L. M. (2020, June 9-12). Decoupled Maximum Constant Boost Control for Quasi-Z-Source Inverter. In: Proceedings of the IEEE International Conference on Environment and Electrical Engineering and IEEE Industrial and Commercial Power Systems Europe (EEEIC / I & CPS Europe), Madrid, Spain. doi:10.1109/EEEIC/ICPSEUROPE49358.2020.9160623

Hong, D., & Cha, H. (2021). LED Current Balancing Scheme Using Current-Fed Quasi-Z-Source Converter. *IEEE Transactions on Power Electronics*, *36*(12), 14187-14194. doi:10.1109/TPEL.2021.3083842

Li, J., Chen, D., & Jiang, J. (2022). Single-Phase ZVS Quasi-Z-Source Inverter with High Voltage Gain. *IEEE Transactions on Power Electronics*, *37*(4), 4346-4357. doi:10.1109/TPEL.2021.3121712

Liu, J., Wu, J., Qiu, J., & Zeng, J. (2019). Switched Z-Source/Quasi-Z-Source DC-DC converters with reduced passive components for photovoltaic systems. *IEEE Access*, *7*, 40893-40903. doi:10.1109/ACCESS.2019.2907300

Mohammadi, M., Mirzaee, A., Magnone, P., Moghani, J., & Mattavelli, P. (2020). Performance improvement of pulse width-amplitude modulation-based quasi-Z-source inverters: Analysis and implementation. *International Journal of Circuit Theory and Applications*, *48*(10), 1786-1799. doi:10.1002/CTA.2808

Nguyen, M.-K., Choi, Y.-O. (2021). Modulation Technique for Modified Active Quasi-Z-Source Inverter with Common-Mode Voltage Reduction. *Electronics*, *10*(23), 2968. doi:10.3390/ELECTRONICS10232968

Padmavathi, P., & Natarajan, S. (2020). Single switch quasi Z-source based high voltage gain DC-DC converter. *International Transactions on Electrical Energy Systems*, *30*(7), e12399. doi:10.1002/2050-7038.12399

Paikray, A., Prudhvi, S., & Nayak, S. K. (2022, December 14-17). Improved Enhanced-Boost Quasi-Z-Source Inverter. In: Proceedings of the 10th IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES-2022), Jaipur, India. doi:10.1109/PEDES56012.2022.10080512

Parla, G., & Özdemir, M. (2022). Design of a Three Phase Z-Source Inverter for Photovoltaic Systems. Dicle University Journal of Engineering, *13*(2), 253-261. doi:10.24012/dumf.1100464

Peng, F. Z. (2002, October 13-18). Z-source inverter. In: Proceedings of the Conference Record of the 2002 IEEE Industry Applications Conference, 37th IAS Annual Meeting, vol. 2, (pp. 775-781), Pittsburgh, USA. doi:10.1109/IAS.2002.1042647

Peng, F. Z. (2003). Z-source inverter. *IEEE Transactions on Industry Applications*, *39*(2), 504-510. doi:10.1109/TIA.2003.808920

Peng, F. Z., Yuan, X., Fang, X., & Qian, Z. (2003). Z-source inverter for adjustable speed drives. *IEEE Power Electronics Letters*, *1*(2), 33-35. doi:10.1109/LPEL.2003.820935

Poorali, B., & Adib, E. (2020). Soft-Switched High Step-Up Quasi-Z-Source DC-DC Converter. *IEEE Transactions on Industrial Electronics*, *67*(6), 4547-4555. doi:10.1109/TIE.2019.2922948

Sabeur, N., Mekhilef, S., & Masaoud, A. (2018). A Simplified Time-Domain Modulation Scheme-Based Maximum Boost Control for Three-Phase Quasi-Z Source Inverters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, *6*(2), 760-769. doi:10.1109/JESTPE.2017.2763974

Sun, D., Ge, B., Bi, D., & Peng, F. Z. (2013). Analysis and control of quasi-Z source inverter with battery for grid-connected PV system. *International Journal of Electrical Power & Energy Systems*, *46*, 234-240. doi:10.1016/J.IJEPES.2012.10.008

Xu, G., Chen, D., & Qu, A. (2020, October 19-21). Simple Boost Modified Space Vector Modulation Strategy for Three-Phase Quasi-Z-Source Inverter. In: Proceedings of the 46th Annual Conference of the IEEE Industrial Electronics Society, (pp. 5365-5370), Singapore. doi:10.1109/IECON43393.2020.9255384

Zhao, Z., Elgendy, M. A., Armstrong, M., & Muhammad, M. (2019, September 3-5). Constant boost control with third harmonic injection for quasi-Z source inverter used in PV grid-connected system. In: Proceedings of the 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe), Genova, Italy. doi:10.23919/EPE.2019.8915379