Osmangazi Üniversitesi Müh. Mim. Fak. Dergisi C.XIII, S.1, 2000
Eng. & Arch. Fac. Osmangazi University, Vol. XIII, No. 1, 2000

Si/SiGe HETEROJUNCTION BIPOLAR TRANSISTORS
(A REVIEW)

Hasan Hüseyin ERKAYA[1]

ABSTRACT: *The research on Si/SiGe heterojunction bipolar transistors has led the ultra-high-speed transistors that are compatible with the state-of-the-art silicon integrated technology. The SiGe base regions of these transistors are grown selectively on silicon substrates. Self-aligned structures are used to reduce the external base resistance and base collector parasitic capacitance. The germanium profile in the base is graded to obtain a drift effect to reduce the base-transit time. Si/SiGe integrated circuits for applications in optical-fiber link systems and Si/SiGe microwave power transistors have been produced with remarkable speeds. The SiGe semiconductor material system, HBT structures and fabrication, and device performance issues are reviewed in this paper.*

KEYWORDS: *SiGe alloys, heterojunction bipolar transistors*

Si/SiGe HETEROJONKSİYON BİPOLAR TRANZİSTÖRLER
(DERLEME)

ÖZET: *Si/SiGe heterojonksiyon tranzistörler konusunda yapılan araştırmalar sonucu, modern yüksek teknoloji kullanan silisyum tümleşik devre üretme teknikleriyle üretilebilen çok yüksek hızlı tranzistörler üretilmektedir. Bu tranzistörlerin baz bölgeleri Si taban üzerine seçmeli SiGe kristal üretme ile gerçekleştirilmekte, aktif bölge dışında kalan baz bağlantı bölgesinin olabildiğince kısa olması ve baz-kollektör parazitik sığasının küçük tutulması için kendinden hizalı yapılar kullanılmaktadır. Baz bölgesi içinde germanyum yüzdesi değişken tutularak azınlık taşıyıcılar için ek bir sürüklenme etkisi oluşturulmakta ve böylece baz geçiş süresi azaltılmaktadır. Fiber-optik uygulamalar için Si/SiGe tümleşik devreler ve Si/SiGe mikrodalga güç transistörleri üretilmiş, çok iyi sonuçlar alınmıştır. Bu yazıda SiGe yarıiletken malzeme sisteminin bazı özellikleri, HBT yapıları ve üretim yöntemleri, ve tranzistör performansı konuları ele alınmıştır.*

ANAHTAR KELİMELER: *SiGe alaşımlar, heterojonksiyon bipolar tranzistörler*

---

[1] *Osmangazi Üniversitesi, MMF Elektrik-Elektronik Mühendisliği Bölümü, Batı Meşelik Kampusu, 26480 ESKİŞEHİR*

I. INTRODUCTION

The first generations of heterojunction bipolar transistors were fabricated about fifteen years after the idea was first introduced by Schockley [1] in 1951 and later elaborated by Kroemer [2] in 1957. Brojdo *et al.* [3] and Page [4] reported CdS/Si transistors in 1965. Jadus [5] produced GaAs/Ge transistors; Hovel and Milnes [6], ZnSe/Ge in 1967. In 1970, Sleger *et al.* [7] reported ZnSe/GaAs heterojunction transistors. All these transistors had current gains of 5 to 70.

There were problems with some of these structures. For instance, in a GaAs/Ge HBT structure, As diffuses into the Ge base layer and converts the conductivity type. Instead of an Npn structure, an N-GaAs/n-Ge/p-Ge/n-Ge structure results from this diffusion [5]. The advances in crystal growth technology have led to the second-generation heterojunction bipolar transistors: AlGaAs/GaAs HBT. In such a structure, a similar diffusion from the emitter into the base would not alter the conductivity type of the base region because Al and Ga are isoelectronic and one can replace the other without altering the conductivity type.

The first AlGaAs/GaAs HBT was reported in 1972 by Dumke et al. [8], and many other researchers produced high-gain AlGaAs/GaAs HBT's. Since the review of HBT's and their potential applications by Kroemer [9] in 1982, the interest in HBTs has skyrocketed. Consequently, many other ternary and quaternary alloy systems have been used for HBT fabrication.

InGaAsP/InP HBTs have been developed for long-wavelength (1-1.6 μm) optical communication and high-speed digital circuit applications [10] -[12]. This alloy system provides higher electron mobility and larger valence band discontinuity than AlGaAs/GaAs system does. The AlGaP/GaP alloy system, too, has been experimented to produce HBTs [13]. This alloy system does not offer high current gain, but it offers transistor operation at elevated temperatures as high as 550°C with a β (common emitter current gain) of 6. Also, AlInAs/InGaAs HBTs have been demonstrated [14] to operate at 4.2 K with a β of 180. AlGaAs/InGaAs/GaAs alloy system, too, has been used to produce strained layer HBTs [15].

Later, a new trend appeared in the fabrication of HBTs: Silicon substrates were used to fabricate HBTs. Some of these HBTs had silicon bases. The emitter layers were made of hydrogenated silicon or a silicon compound: α-Si:H [16], α-SiC:H [17] or β-SiC [18]. The other HBTs on silicon substrates had GaAs bases and AlGaAs emitters. This

so-called "GaAs on Si" material system allows GaAs and Si devices to be combined on a monolithic circuit. It also provides larger and less fragile wafers and higher thermal conductivity than GaAs alone does. The effects of the large mismatch (4%) between GaAs and Si are eliminated by various techniques including the growth of a thick graded layer.

While the III-V heterojunction bipolar transistors are on their way to maturity, a relatively new heterostructure has been experimented for bipolar transistors: Si/SiGe/Si [19]-[21]. This system, too, uses silicon wafers and is compatible with the existing silicon technology. There are reports of excellent device performance such as a cutoff frequency of 130 GHz [22] and gate delays of 9.3 ps in ECL gates [23].

The SiGe semiconductor material system, HBT fabrication, and device performance issues will be reviewed in this paper.

I.1 Si-Ge Alloy

Silicon and germanium can be mixed to produce the alloy $Si_{1-x}Ge_x$ for the entire compositional range $0 < x < 1$. The alloy has the diamond crystal structure and its lattice constant is a linear function of the germanium fraction [24] as

$$a(Si_{1-x}Ge_x) = a(Si) + [a(Ge) - a(Si)]\, x \qquad (1)$$

or with numerical values,

$$a(Si_{1-x}Ge_x) = 0.54307 + 0.02268\, x \text{ [nm]} \qquad (2)$$

for low values of x. The room temperature mismatch between germanium and silicon is 4.17 % that increases slightly with temperature. When Si-Ge alloy is grown on a thick Si substrate, the mismatch will cause non-uniformity in the lattice. Depending on the growth conditions and the thickness of the grown layer, the mismatch may be accommodated by the production of misfit dislocations at the interface or by the tetragonal distortion of the lattice.

If the misfit dislocations are allowed during the growth, the lattice will be relaxed or unstrained. The dislocations may be positioned at the interface or threaded through the grown layer. When the misfit dislocations are not formed, the lattice constant in the direction perpendicular to the substrate will be different from the lattice constant in the

plane of the substrate surface. This creates strain in the grown layer, so the lattice is called strained lattice; the growth, pseudomorphic growth.

I.2 Band Gap

The band gap of the SiGe alloy depends not only on the fraction of germanium but also on the presence of strain. In the absence of strain, the band structure of the alloy resembles that of silicon for a germanium fraction below 85 atomic percent. The smallest gap occurs near the X Brillouin zone boundary. For larger germanium fractions, the band structure is germanium-like, and the smallest indirect gap occurs near the L Brillouin zone boundary [24]. The energy gap of the unstrained bulk alloy, which is shown in Figure 1, may be approximated with three line segments. The empirical expressions for the band gap of the unstrained $Si_{1-x}Ge_x$ at 90 K are as follow:

$$E_g(x) = \begin{cases} 1.17 - 0.44x & eV \quad for \quad 0 < x < 0.35 \\ 1.05 - 0.1x & eV \quad for \quad 0.35 < x < 0.85 \\ 0.95 - 1.5(x - 0.85) & eV \quad for \quad 0.85 < x < 1.0 \end{cases} \tag{3}$$

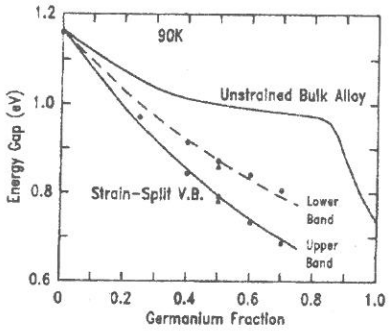

Figure 1. The energy band gap of unstrained and pseudomorphic SiGe alloys [24]. The pseudomorphic alloy is grown on a silicon substrate.

Figure 1 also shows the energy gap of pseudomorphic SiGe grown on silicon substrate. The band gap of strained $Si_{1-x}Ge_x$ on silicon substrate at 90 K may be expressed as

$$E_g(x) \approx 1.17 \exp(-0.8x) \text{ eV} \quad \text{for } 0 < x < 0.7 \tag{4}$$

The room temperature band gap is slightly smaller for the same germanium fraction for the strained alloy grown on (100) silicon substrate [25]:

$$E_g(x) = 1.12 - 0.74x \text{ eV} \quad (5)$$

The comparison of the curves in Figure 1 indicates that the presence of tetragonal strain significantly reduces the energy gap. The strain-split heavy hole band determines the smallest gap in the band structure. The band gap of the pseudomorphic alloy on silicon substrate can be smaller than the band gap of germanium for $x > 0.6$.

Growing strained $Si_{1-x}Ge_x$ on unstrained SiGe substrate is also possible. Depending on both the composition of the substrate and the composition of the pseudomorphic layer, a different value of the band gap will be obtained. Figure 2 displays the composition dependence of the band gap of $Si_{1-x}Ge_x$ layers on four different substrates [24].

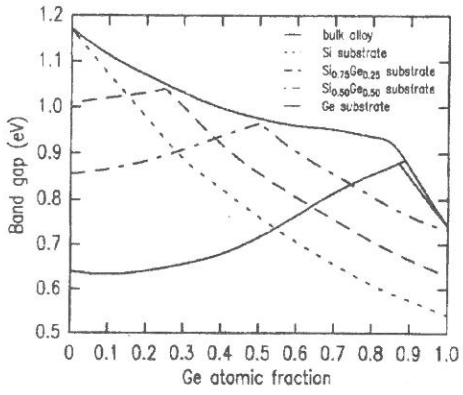

Figure 2. The energy band gap of pseudomorphic SiGe alloy grown on different substrates [24].

The band alignments and band offsets between the silicon and SiGe alloy depend on the relative strains in the heterostructure. The strained Si layer grown on unstrained $Si_{0.5}Ge_{0.5}$ substrate, for instance, forms a type II alignment [24]. The valence band discontinuity for the pseudomorphic $Si_{1-x}Ge_x$ on silicon is given in Figure 3. Theoretical calculations and experimentally extracted values are included in the same figure [26]. The conduction band discontinuity for the strained alloy on silicon substrate is given in Figure 4. The conduction band discontinuity is much smaller than the valence band discontinuity for a given germanium fraction; hence, the valance band discontinuity may be approximated by the total band-gap difference.

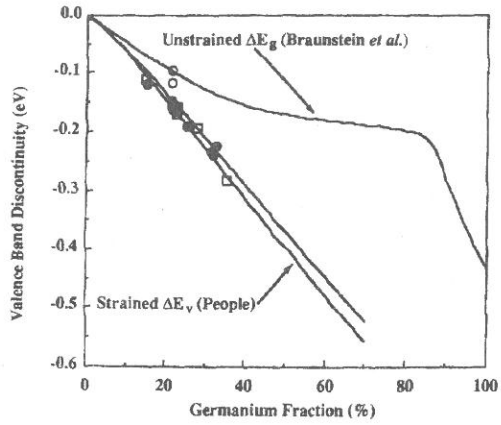

Figure 3. The valence band discontinuity between the pseudomorphic SiGe alloy and silicon substrate [26].

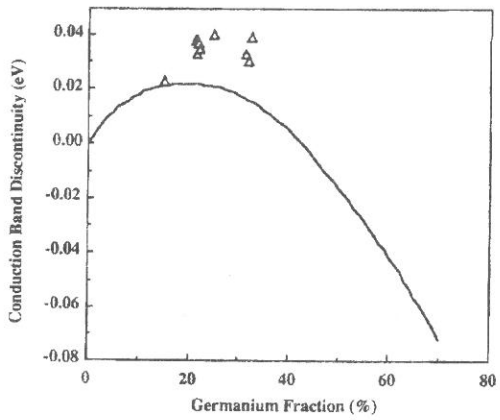

Figure 4. Conduction band discontinuity between the pseudomorphic SiGe alloy and silicon substrate [26]

II. CRYSTAL GROWTH

During the growth of the pseudomorphic SiGe alloy on silicon substrate, care must be taken so that the strain in the lattice is not relaxed to result in misfit dislocations. The same care must be maintained during the processing of the grown layers for device fabrication. For instance, the exposure to high temperatures will be detrimental for the

pseudomorphic layer. Also, the thickness of the grown layer should not exceed the critical thickness.

For quality epitaxial growth, the atomic mobility at the growth surface must be high. This mobility increases with increasing temperature, making high temperature growth desirable. On the other hand, islanding and strain relaxation by dislocation nucleation, too, are enhanced at high temperatures resulting in poor epitaxial growth. Hence an optimum growth temperature has to be found. Since, the strain in the lattice depends on the germanium fraction of the alloy, the optimum growth temperature depends on the germanium fraction, too. For "moderate" Ge fraction, which is below 15 atomic percent, the optimum growth temperature is about 550 °C [24].

The thickness of the epitaxially grown SiGe layer on a silicon substrate is another factor affecting the strain in the alloy. For the pseudomorphic growth, the layer thickness must be smaller than the critical thickness that depends on the germanium fraction. Figure 5 displays the critical thickness versus the germanium fraction. The theoretical curves and some experimental values are given in the same figure. Iyer *et al.* [24] suggest that the substrate preparation, the use of buffer layers, and the particulate contamination during the epitaxial growth are the practical key factors to affect the dislocation formation, and hence, the critical thickness.

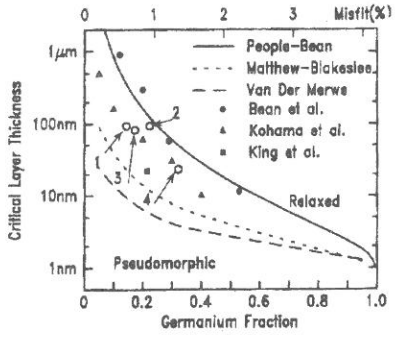

Figure 5. Critical thickness for the pseudomorphic SiGe alloy grown on silicon substrate [24]

There are two common basic methods of growing pseudomorphic SiGe alloys on Si substrates: Molecular-beam epitaxy (MBE) and chemical vapor deposition (CVD).

II.1 Molecular-Beam Epitaxy

In the MBE growth of the pseudomorphic SiGe alloys the substrate is heated to the proper temperature, and elemental Si, Ge and dopant sources are used. In general, Ga is used for p-type doping while Sb is used for n-type doping. The spontaneous incorporation of these dopants from the flux does not happen; instead, an adlayer of the dopant is formed at the growth surface. In case of Sb, the adlayer is bombarded with low energy Si+ ions that cause the secondary implantation of Sb atoms into the alloy. This also creates some point defects in the layer that complicates the growth [24].

For the doping of MBE grown layers several other techniques are also used. For instance B is incorporated from the flux through a complex process. Direct implantation and solid phase crystallization techniques are other doping techniques. Both n-type and p-type doping up to 10^{20} cm^{-3} with a sharp profile is achievable in MBE growth techniques [24].

II.2 Chemical Vapor Deposition

For the CVD growth of the SiGe on silicon substrates, ultrahigh-vacuum/chemical vapor deposition (UHV/CVD) is used [24]. Initial substrate surface cleaning and the maintenance of the high-purity environment during the growth are key issues in this technique. The traditional high temperature (above 1000°C) cleaning is not proper for the pseudomorphic SiGe; the growth temperature is around 550°C. Also, high vacuum (0.001 mbar) is needed for the proper adherence of the grown layer to the substrate. The deposition takes place through the heterogeneous prolysis of silane, germane, and diborane.

Another CVD technique is the limited-reaction processing (LRP) [24], [26]. In this technique, a single substrate is radiatively heated in a cold-wall system in vacuum (1 mtorr). The sources are dicholorosilane, germane and diborane. The initial cleaning is carried out at 1200°C in hydrogen ambiance, and then a 1-2 μm thick Si-buffer layer is grown. The growth of the pseudomorphic SiGe follows at 640°C. The growth rate is given in Figure 6.

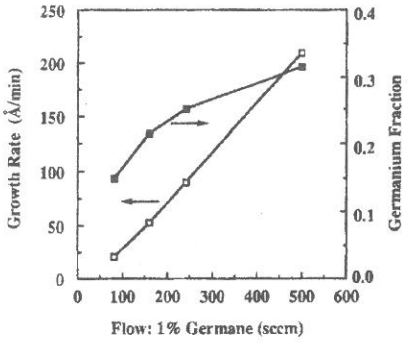

Figure 6. Pseudomorphic SiGe growth rate [26]

All three of these techniques produce sufficiently high-quality crystals for device fabrication.

III. DEVICE FABRICATION

The MBE and CVD grown heterostructures are processed to form the HBTs. During the processing steps the strain in the lattice has to be preserved. This prohibits processing steps that require high temperatures. For instance, deposited oxides are used rather than the thermally grown oxides. Also rapid thermal annealing is used rather than the traditional furnace annealing.

The SiGe device structure may be classified into three categories: mesa structures, non-self-aligned structures and self-aligned structures [27]. While the growth of SiGe layer takes place over the entire wafer in the mesa structures, selective crystal growth over the substrate is required for the non-mesa structures.

III.1 Mesa Structures

The mesa structures used in III-V technology were borrowed for the fabrication of early SiGe heterojunction bipolar transistors. Various mesa structures are formed for emitter/base definition or for device isolation. A mesa defined transistor structure is given in Figure 7. In this structure dry etching is used to define the mesa. The base contact resistance is reduced with Ga implantation below the contact. The passivation for the surface is accomplished with a low temperature oxide deposition. A mesa isolated device structure is given in Figure 8. In this structure, the active device has a completely planar structure while a mesa is formed for isolation. The base layer is

reached from the surface with a boron implant with a deposited oxide mask. An As implant is carried out for the emitter contact. The devices pictured in Figure 7 and Figure 8 have single crystal emitters.

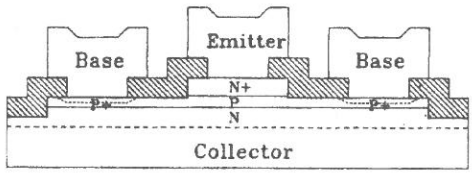

Figure 7. Mesa defined transistor structure [24]

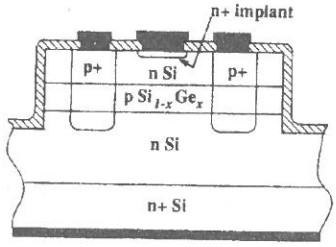

Figure 8. Mesa isolated planar transistor structure [26]

III.2 Non-Self-Aligned Structures

The non-self aligned structures may be grouped into three: simple emitter window, extrinsic base before SiGe base epitaxy, and extrinsic base after SiGe base epitaxy [27]. In the first group, the base layer is grown immediately after isolation processes. An oxide/nitride passivation layer is deposited over the base layer. Then, the emitter windows are opened. The region of the base layer extending over the isolation layers could be used to contact the base, yet the thickness and the doping level would be insufficient for low external resistance. The single-crystal base layer can be reached for contact from the top, yet that would require larger isolation window at the expense of increased base-collector junction area. Another major drawback of this type of structure is that the base layer is subject to all subsequent thermal processes.

To reduce the external base resistance, a heavily doped polysilicon is formed immediately before the growth of SiGe base layer. A window is opened for the intrinsic base. After the base growth, oxide/nitride passivation layer is formed. Then emitter windows are opened. The structure is complete with the deposition of n+ polysilicon

for the emitter. Such a transistor structure is given in Figure 9. In this structure the p+ poly layer under the SiGe base layer reduces the external base resistance and provides low-resistance contact for the base.

In the third group of non-self aligned structures, the extrinsic base layer is formed after the SiGe layer growth. The structure can be described as a blend of other two non-self-aligned structures.

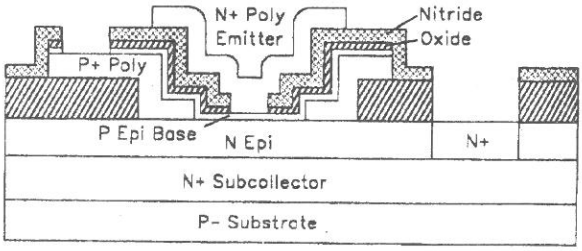

Fig. 17. Schematic cross section of the non-self-aligned bipolar structure with a base formed by UHV/CVD low-temperature epitaxy [107].

Figure 9. Schematic cross section of a non-self-aligned bipolar transistor structure [24]

III.3 Self-Aligned Structures

New structures were developed to reduce the total base resistance and the base-collector junction capacitance. These techniques aim at reducing the lateral distance the base current has to travel and minimizing the base/collector junction area. There are four main types of self aligned structures [27]: (a) Mesa-like structure, (b) Epi-SiGe-base after extrinsic base in a predefined emitter opening, (c) Extrinsic base after epi-SiGe-base overgrowing a pre-defined emitter pad, and (d) Disposable emitter mandrel.

In mesa-like structures, the SiGe base layer is grown over the entire wafer area. Then the base mesa is formed. The complete mesa-like self-aligned structure is given in Figure 10. In this device, the pseudomorphic base layer undergoes two relatively high temperature processes: external base growth and emitter drive-in cycles.

The second self-aligned structure type, epi-SiGe-base after extrinsic base in emitter window, is an extension of the "implanted-base double-poly self-aligned" bipolar technology. The intrinsic epi-SiGe-base is grown selectively in an emitter window using a low-temperature growth process. A finished device structure is given in Figure 11. To obtain this structure, first a thermal oxide is grown over the entire wafer. Then p+ polysilicon is deposited and boron-implanted to obtain a low sheet resistance. Third, a Si_3N_4 deposition is carried out to pattern the p+ polysilicon to form the external base.

After the pattern etching, another deposition and etch-back is carried out to form the Si_3N_4 sidewall. Then, the oxide is removed through the patterned p+ polysilicon window to expose the silicon substrate surface and to produce an overhanging p+ poly edge. The selective growth of polysilicon under the overhanging structure and the selective growth of SiGe base over the substrate surface take place at the same time. When the poly touches the SiGe base, the growth is stopped. Before the deposition of the emitter polysilicon, a borosilicate glass sidewall is formed in the window [28].

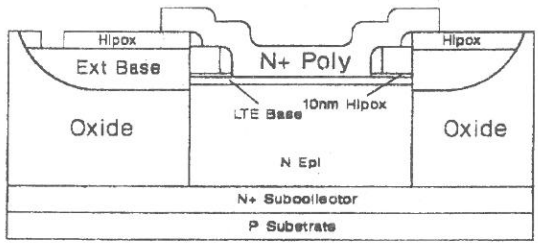

Figure 10. A self-aligned mesa HBT structure [27]

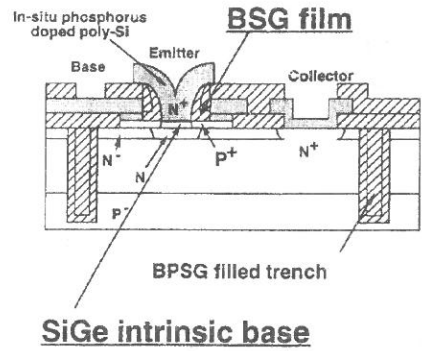

Figure 11. A "super self-aligned" selectively grown SiGe-base HBT cross-sectional view [28].

In the third self-aligned structure, the external base is formed after the SiGe base growth. The structure is also known as *SEEW--Selective-Epi Emitter Window* structure. The self-alignment is achieved by the "selective epi lateral overgrowth over a thin nitride/oxide emitter pad and subsequent oxidation to form the emitter window and the bulk of the extrinsic base layer simultaneously" [27]. The extrinsic base link resistance can be reduced with boron implantation. The SiGe base layer is subject to all thermal cycles required for the extrinsic base processes.

The final self-aligned structure, disposable emitter mandrel, is an extension of the conventional implanted-base single-poly self aligned structure. This structure is the bipolar section of a BiCMOS basic structure [27], [29]. The devices are formed on a p+ wafer with a p- epi layer. First the buried n+ subcollector is formed, and a thin layer of n-type silicon is grown everywhere. This is followed by polysilicon-filled deep trench device isolation and oxide-filled shallow base isolation. Next, a deep phosphorus diffusion is formed to reach the buried collector layer from the surface. After this diffusion, p-well and n-well are implanted and annealed. Then a thin gate oxide is grown. This oxide is protected with a polysilicon layer. Later, this polysilicon is patterned to expose the bipolar transistor area. SiGe base layer is grown over the entire surface. The region over the exposed silicon grows pseudomorphic while the rest of the areas grow poly. These poly regions serve as external base contacts or gate electrodes for the MOSFETs. Following the base growth, a passivation oxide is grown using low temperature HIPOX to minimize base dopant diffusion. Then, a thin layer of nitride and a thin layer of polysilicon "conversion layer" are deposited. The emitter "mandrel" is formed with the deposition and patterning of PECVD nitride and thick PECVD oxide layers. This mandrel is used to block the high-dose extrinsic base boron implant. After the base implant, this mandrel is removed to leave a window for the emitter. In the final steps, polysilicon is deposited, implanted and patterned for the emitter contact. For the patterning of the base and the gates, highly selective etches are used. Self-aligned titanium disilicide was formed over the extrinsic base poly and the gates, and salicidation of the extrinsic base is carried out to reduce overall base resistance. The structure of a finished device is given in Figure 12.

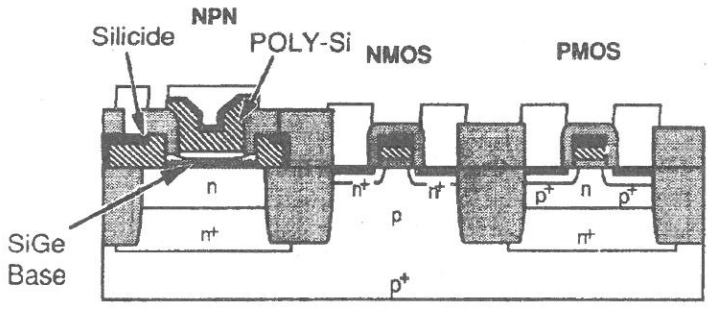

Figure 12. BiCMOS device structure with SiGe-base transistor [29]

III.4 An Alternative Approach

As an alternative to the crystal growth with MBE or CVD, Ge implantation in Si is used to form the $Si_{1-x}Ge_x$ base layer. Lombardo *et al.* [30]-[31] fabricated such npn bipolar transistors with high dose of Ge implant. A rapid thermal anneal at 1000°C for 10 s in nitrogen ambient was sufficient to restore the crystal. The wafers are processed with the standard self-aligned, double polysilicon process. They demonstrated that a high-dose Ge implantation in the base improved the current gain, base resistance, and forward transit time for the silicon transistors.

III.5 Some Fabrication Issues

There have been many issues regarding the commercial production of SiGe HBTs. Some of these issues are related to the crystal growth whereas some are related to the integration with the state-of-the-art silicon integrated circuit technology.

One of the problems with the crystal growth is the surface preparation of the silicon substrate. If a blanket growth is required over bare silicon, the surface preparation is relatively easy. A 10-second dip in dilute HF:H_2O (1:10) is sufficient for the hydrogen passivation of the growth surface. The wafers may be loaded to the growth chamber without blow-drying. If the wafer is patterned and a selective growth is required, then additional precautions must be taken. For instance, oxide regions have to be protected by an additional layer of polysilicon. Also blow-drying is needed for the patterned wafer. Some structures may prevent wet passivation of the surfaces.

Another problem with the base layer is the dopant out diffusion. Since very high levels of doping is used in the thin base layer, some out diffusion of the base dopant during the consequent process steps at elevated temperatures is unavoidable. Undoped spacers are used to prevent the diffusion front from reaching the collector and emitter layers.

A third problem with the base layer is the maintenance of the strain in the layer. Although the critical thickness is not reached for the initial base growth, the high-temperature exposure will cause the formation and propagation of defects at the interfaces. This will cause a partial relaxation of the strain in the base and provide recombination centers.

Despite all of these problems, excellent Si/SiGe heterojunction bipolar transistors have been produced with some modifications of the state-of-the-art silicon integrated circuit technology.

IV. DEVICE PERFORMANCE

The initial research on Si/SiGe heterojunction bipolar transistors aimed at the demonstration of better intrinsic transistor characteristics such as the common emitter current gain, Early voltage, and cutoff frequency. Later, optimum device design concepts were developed. The germanium profile in the base is optimized for various purposes. Finally, large-scale integration issues were focused. Self-aligned silicon device structures have been modified to incorporate the SiGe base into the current technology. The outcome is very pleasing.

The performance of a transistor is evaluated using several figures of merit such as common emitter current gain (□), unity-gain cutoff frequency (f_T) and ECL gate-delay. Due to the reduced band gap in the base, very high values of current gain is easily achievable with SiGe heterojunction transistors. For example, a β of 29000 was reported by Oda *et al.* [33]. Also temperature dependence of the current gain reveals that SiGe HBTs keep their high gain at lowered temperatures as well (Figure 13). Grading the band gap in the base provides a drift field that improves the gain, cutoff frequency and Early voltage. However, the reduced band gap in the base also lovers the breakdown voltage for the base collector junction. A record high f_T of 130 GHz has been reported by Oda et al.[22], [32]. A comparison of the reported cutoff frequencies of the SiGe base and Si base bipolar transistors is given in Figure 14. It is clear from the figure that the SiGe base heterojunction bipolar transistors have about 50% higher cutoff frequencies [33].

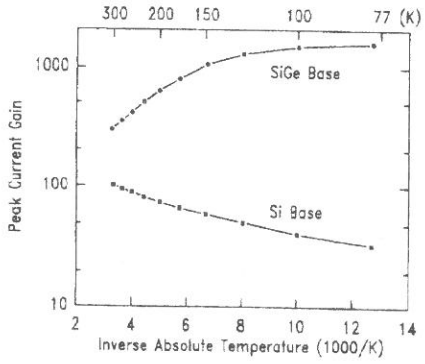

Figure 13. Temperature dependence of current gain for Si- and SiGe-base devices formed by UHV/CVD low-temperature epitaxy [24].

The improvements in the device parasitics also reduced the gate delay of ECL circuits. For instance, Washio reported "ultra-high-speed" ECL circuit with an 8.0 ps gate-delay [34]. The gate delay time trends for ECL circuits over last two decades are given in Figure 15 for comparison among bipolar technologies. These transistors have been used in integrated circuits for optical-fiber link systems. Examples of such integrated circuits include a 1/8 static frequency divider operating at 50 GHz, a time-division multiplexer and a demultiplexer operating at 40 Gb/s, a preamplifier with a 35 GHz bandwidth, and a decision circuit operating at 40 Gb/s [34].

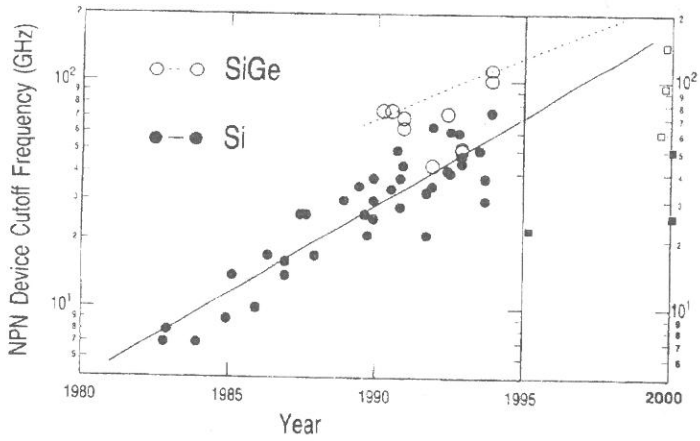

Figure 14. Si and SiGe device performance over the past years. (The year scale of the original graph by Warnock [33] has been extended to 2000. The solid squares are for Si devices; blank squares, for SiGe devices.)

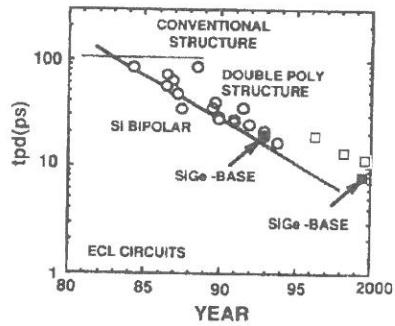

Figure 15. Gate delay time trends for ECL circuits [29]. (Data for the years between 1995 and 2000 have been added to the original graph by Nakamura and Nishizawa [29]. The blank squares are for Si devices; solid squares, for SiGe devices.)

There have also been power applications of SiGe-base heterojunction transistors. Schuppen *et al.* [35] reported 1-W SiGe power HBT for wireless communication. Potyraj *et al.* [36] fabricated 230-watt S-band SiGe power transistor operating in Class C. Recently Z. Jinshu *et al.* [37] reported 5-W SiGe HBT which had 60 emitter stripes and no emitter ballasting resistors.

V. CONCLUSION

The research on Si/SiGe heterojunction bipolar transistors has led the ultra-high-speed transistors that are compatible with the state-of-the-art silicon integrated technology. The SiGe base regions of these transistors are grown selectively on silicon substrates. Self-aligned structures are used to reduce the external base resistance and base collector parasitic capacitance. The germanium profile in the base is graded to obtain a drift effect to reduce the base-transit time. Si/SiGe integrated circuits for applications in optical-fiber link systems and Si/SiGe microwave power transistors have been produced with remarkable speeds.

REFERENCES

[1] W. Shockley, U. S. Patent no: 2 569 347, Sep. 1951.

[2] H. Kroemer, "Theory of a wide-gap emitter for transistors," *Proc. IRE*, vol. 45, no. 11, pp. 1535-1537, Nov. 1957.

[3] S. Brojdo, T. J. Riley, and G. T. Wright, "The heterojunction transistor and the space charge-limited triode," *Brit . Appl. Phys.*, vol. 16, no. 2, p. 133, Feb. 1965.

[4] D. J. Page, "A CdS-Si heterojunction transistor," *IEEE Trans. Electron Devices*, vol. ED-12, no. 9, pp. 509-510, Sep. 1955.

[5] D. K. Jadus, "The realization of a wide band gap emitter transistor," Ph.D. Thesis, Carnegie-Mellon University, Pittsburgh, Pennsylvania, 1957, also, D. K. Jadus and D. L. Feucht, "The realization of a wide band gap emitter transistor," *IEEE Trans. Electron Devices*, vol. ED-15, no. 1, p. 102, Jan. 1959.

[6] H. J. Hovel and A. G. Milnes, "ZnSe-Ge heterojunction transistors," *IEEE Trans. Electron Devices*, vol. ED-15, no. 9, p. 755, Sep. 1969.

[7] K. Sleger, A. G. Milnes, and D. L. Feucht, "ZnSe-GaAs and ZnSe-Ge heterojunction transistors, *Proc. Int. Conf. Phys. Chem. Semicond. Heterojunctions Layer Structures* (Budapest), vol. 1, p.73, 1970, also, K. Sleger,

"ZnSe-GaAs Heterojunction Transistors," Ph.D. Thesis, Carnegie-Mellon University, Pittsburgh, Pennsylvania, 1971.

[8] W. P. Dumke, J.M. Woodall, and V. L. Rideout, "GaAs-GaAlAs heterojunction transistor for high frequency operation," *Solid-State Electronics*, vol. 15, no. 10, pp. 1339-1343, Oct. 1972.

[9] H. Kroemer, "Heterojunction bipolar transistors and integrated circuits," *Proc. IEEE*, vol. 70, no.l, pp. 13-25, Jan. 1982.

[10] L. M. Su, N. Grote, R. Kaumanns, W. Katzschner, and H. G. Bach, "An InGaAsP/InP double-heterojunction bipolar transistor for monolithic integration with a 1.5-μm laser diode," *IEEE Electron Device Lett.*, vol. EDL-6, no. 1, pp. 14-17, Jan. 1985

[11] N. Grote, L. M. Su, and H.-G. Bach, "Characteristics of double-heterojunction InGaAsP/InP bipolar transistors," in *Proc. Symp. GaAs and Related Compounds*, pp. 583-588, 1985.

[12] H. Fukano, Y. Itaya, and G. Motosugi, "InGaAsP/InP heterojunction bipolar transistor with high current gain," *Jpn. J. Appl. Phys.* Part 2, vol. 25, no. 6, pp. L504-L506, June 1986.

[13] T. E. Zipperian and L. R Dawson, "GaP/$Al_xGa_{1-x}P$ heterojunction transistors for high-temperature electronic applications," *J. Appl. Phys.*, vol. 54, no. 10, pp. 6019-6025, Oct. 1983.

[14] A. Furukawa and T. Baba, "4.2 K operation of a InAlAs/InGaAs heterojunction bipolar transistor," *Jpn. J. Appl. Phys.* Part 2, vol. 25, no. 10, pp. L862-L864, Oct. 1985.

[15] G. J. Sullivan, P. M. Asbeck, M. F. Chang, D. L. Miller, and K. C. Wang, "AlGaAs /InGaAs /GaAs strained-layer heterojunction bipolar transistors by molecular beam epitaxy," *Electron. Lett.*, vol. 22, no. 8, pp. 419-421, 10 Apr. 1986.

[16] M. Ghannam, J. Nijs, R. Mertens, and R. DeKeersmaecker, "A silicon bipolar transistor with a hydrogenated amorphous emitter," in *IEDM Tech. Dig.*, pp. 746-748, 1984.

[17] K. Sasakir S. Furukawa, and M. M. Rahmanr, "A novel structure amorphous SiC:H emitter HBT using low temperature process," in *IEDM Tech. Dig.*, pp. 294-297, 1985.

[18] T. Sugii, T. Ito, Y. Furumura, M. Doki, F. Mieno, and M. Maeda, "□-SiC/Si heterojunction bipolar transistors with high current gain," *IEEE Electron Device Lett.*, vol. EDL-9, no. 2, pp. 87-89, Feb. 1988.

[19] G. L. Patton, S. S. Iyer, S. L. Delage, S. Tiwari, and J.M.C. Stork, "Silicon-germanium-base heterojunction bipolar transistors by molecular beam epitaxy," *IEEE Electron Device Lett.*, vol. EDL-9, no. 4, pp. 165-167, April 1988

[20] J. F. Gibbons, C. A. King, J. L. Hoyt, D. B. Noble, C. M. Gronet, M. P. Scott, S. J. Rosner, G. Reid, S. Laderman, K. Nauka, J. Turner, and T. I. Kamins, "Si/$Si_{1-x}Ge_x$ heterojunction bipolar transistors fabricated by limited reaction processing," in *IDEM, Tech. Dig.*, 1988, pp. 566-569.

[21] C. A. King, J. L. Hoyt, C. M. Gronet, J. F. Gibbons, M. P. Scott, and J. Turner, "Si/$Si_{1-x}Ge_x$ heterojunction bipolar transistors fabricated by limited reaction processing," *IEEE Electron Device Lett.*, vol. EDL-10, no. 2, pp. 52-54, February 1989

[22] K. Oda, E. Ohue, M. Tanabe, T. Onai, and K. Washio, "130 GHz f_T SiGe HBT technology," in *IDEM, Tech. Dig.*, 1997, pp. 791-794.

[23] K. Washio, E. Ohue, K. Oda, M. Tanabe, H. Shimamoto, T. Onai, and M. Kondo, "A selective-epitaxial-growth SiGe-base HBT with SMI electrodes featuring 9.3-ps ECL-gate delay," *IEEE Trans. Electron Devices*, V.46, no. 7, pp 1411-1416, July 1999.

[24] S. S. Iyer, G. L. Patton, J. M. C. Stork, B. S. Meyerson, and D. L. Harame, "Heterojunction bipolar transistors using Si-Ge alloys," *IEEE Trans. Electron Devices,* V.36, no. 10, pp 2043-2064, Oct 1989.

[25] B. Pejcinovic, L. E. Kay, T. W. Tang, and D. H. Navon, "Numerical simulation and comparison of Si BJT's and $Si_{1-x}Ge_x$ HBT's," *IEEE Trans. Electron Devices,* V.36, no. 10, pp 2129-2137, Oct 1989.

[26] C. A. King, J. L. Hoyt, and J. F. Gibbons, "Bandgap and transport properties of $Si_{1-x}Ge_x$ by analysis of nearly ideal Si/$Si_{1-x}Ge_x$/Si heterojunction bipolar transistors," *IEEE Trans. Electron Devices,* V.36, no. 10, pp 2093-2104, Oct 1989.

[27] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J.Y.-C. Sun, b. S. Meyerson, and T. Tice, "Si/SiGe Epitaxial-base transistors--Part II: Process integration and analog applications," *IEEE Trans. Electron Devices.*, vol. 42, no. 3, pp. 469-482, March 1995

[28] S. Fuhimiko, T. Hashimoto, T. Tatsumi, and T. Tashiro, "Sub-20ps ECL circuits with high-performance super self-aligned selectively grown SiGe base (SSSB) bipolar transistors," *IEEE Trans. Electron Devices.*, vol. 42, no. 3, pp. 390-398, March 1995

[29] T. Nakamura and H. Nishizawa, "Recent progress in bipolar transistor technology," *IEEE Trans. Electron Devices.*, vol. 42, no. 3, pp. 483-488, March 1995

[30] S. Lombardo, A. Pinto, V. Raineri, P. Ward, G. La Rosa, G. Privitera, and S. U. Campisano, "Si/Ge_xSi_{1-x} heterojunction Bipolar Transistors with the Ge_xSi_{1-x} base formed by Ge ion implantation in Si," *IEEE Electron Dev Lett.*, vol. 17, no. 10, pp. 485-487, October 1996

[31] S. A. Lombardo, V. Privitera, A. Pinto, P. Ward, G. La Rosa, and S. U. Campisano, "Band -gap narrowing and high-frequency characteristics of Si/Ge_xSi_{1-x} heterojunction Bipolar Transistors formed by Ge ion implantation in Si," *IEEE Trans. Electron Devices.*, vol. 45, no. 7, pp. 1531-1537, July 1998

[32] K. Oda, E. Ohue, M. Tanabe, H. Shimamoto, and K. Washio, "DC and AC performances in selectively grown SiGe-base HBTs," *IEICE Trans. on Electronics*, vol. E82C, no. 11, pp. 2013-2020, November 1999

[33] J. D. Warnock, "Silicon bipolar device structures for digital applications: Technology trends and future directions," *IEEE Trans. Electron Devices.*, vol. 42, no. 3, pp. 377-389, March 1995

[34] K. Washio, "SiGe HBTs and ICs for optical-fiber communication systems," *Solid-State Electronics*, vol. 43, no. 8, pp. 1619-1625, August 1999.

[35] A. Shuppen, S. Gerlach, H. Dietrich, D. Wandrei, U. seiler, and U. Koenig, "1-W SiGe power HBT's for mobile communication," *IEEE Microwave Guided Wave Lett.*, vol. 6, pp. 341-343, September 1996

[36] P. A. Potyraj, K.J. Petrosky, K.D. Hobart, F. J. Kub, and P. E. Thompson, "A 230-W s-band SiGe heterojunction bipolar transistor," *IEEE Trans. Microwave Theory Tech.*, vol. 44, no. 12, pp. 2392-2397, December 1996

[37] J. Zhang, H. Jia, P.-H. Tsien, and T.-C. Lo, "Emitter-ballasting-resistor-free SiGe microwave power heterojunction bipolar transistor," *IEEE Electron Device Lett.* , vol. 20, no. 7, pp. 326-328, July 1999