ULTRA-LOW VOLTAGE VDBA DESIGN BY USING PMOS DTMOS TRANSISTORS

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Abstract: *In this study, a new ultra-low voltage and ultra-low power voltage differencing buffered amplifier (VDBA) based on dynamic threshold voltage MOS transistors (DTMOS) is proposed. A voltage mode filter configuration is also presented as an application for the proposed VDBA. This filter employed two VDBA blocks and two passive components. The total power consumption of VDBA block is found simply 6.22 nW at a 0.4 V supply voltage. The simulation results by using LTSpice Program with 0.18 µm TSMC CMOS technology model parameters are carried out to show the performance of the proposed active device and its filter applications.*
Keywords: *VDBA, DTMOS, Low Voltage, Filter.*

1. Introduction

The growing demand for ultra-low voltage (ULV), ultra-low power (ULP) and high performance electronic devices and VLSI circuits are attracting significant interest for the scientists and special markets and they have grown rapidly. Power consumption is an important criterion for the continued development of the microelectronic technology [1]. The power consumption has been concerned as a critical parameter particularly for portable electronic devices, medical electronics implant devices and battery powered devices. Dropping the power dissipation of the circuit is necessary to keep battery life much longer than usual. Reducing the power dissipation is easily and effectively possible by lowering the power supply voltage, however, dropping the supply voltage is causing some problems due to the CMOS evolution. One of them is the signal headroom becomes too small to design circuits with sufficient signal integrity and the other problem is the gate leakage [2]. These problems are hindering the designing ULV and ULP electronic devices. These problems can be fixed by using the DTMOS transistors.

Several analog signal processing and signal generation circuits have been designed by the current-mode techniques. Various number of active elements, detailed reviews are given in [3], have been proposed based on different applications. These active elements were designed with either changing the input or output terminal, or changing the control parameter as external current or voltage. These active elements were designed by modifying, reshaping or manipulating the basic elements such as voltage feedback amplifiers, current feedback amplifiers, transconductance amplifiers and current conveyors. The literature surveys show that considerable amount of current mode filters using different type of active blocks have been proposed by several authors. These reported realizations including different active building blocks such as Current Differencing Buffered Amplifiers (CDBAs) [3–6], first generation Current Conveyors (CCI), second generation Current Conveyors (CCIIs) [7–12], Operational Transconductance Amplifiers (OTAs) [13–15], Differential Voltage Current Conveyors (DVCCs) [16–18] and Current Differencing Transconductance Amplifiers (CDTAs) [3,19–24]. The Current Differencing Buffered Amplifier (CDBA) was firstly proposed by Acar and Ozoguz in 1999 [5]. The Voltage Differencing Buffered Amplifier, namely VDBA, which has low output impedance and high input impadence, is proposed in [3] as an alternative to the CDBA. The only differences between the CDBA and VDBA are the signal types of inputs. While input terminals of the VDBA are voltage, the input terminals of the CDBA are current. Fully Balanced Voltage Differencing Buffered Amplifier (FB-VDBA) was firstly published by Biolek and others in [25]. In [26], the new CMOS realization of VDBA and its filter applications was proposed. In this circuit, it needs 3V supply voltage and its power consumption is 0.97 mW.

In this study, the dynamic threshold voltage metal oxides semiconductor (DTMOS) transistors based VDBA circuit and its new filter application is proposed. The circuit can be performed by an ultra-low supply voltage 0.4 V and it is total power consumption is only 6.22 nW. The transistors have been used in weak inversion for the purpose of the

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lower power consumption. Because of their well subthreshold slope characteristic, the DTMOS transistors are very desirable for working under the ultra-low voltages. It is seen from the simulation results both proposed VDBA and the filters have performed very well. The proposed DTMOS-based VDBA circuit is appropriate for ULV and ULP biomedical and analog signal processing applications.

2. DTMOS Based VDBA Design

Assaderaghi and others proposed the Dynamic Threshold voltage MOSFET (DTMOS) for silicon on insulator (SOI) process technology [27–29] in 1994. As shown in Figure 1 [30], the body terminal of the transistor is tied to gate terminal to generate the DTMOS whose threshold voltage utilizing the relation in Eq. 1;

$$V_{TH} = V_{TO} + \gamma\left(\sqrt{\phi_0 + V_{SB}} - \sqrt{\phi_0}\right) \quad (1)$$

where where ϕ_0 is the total surface band bending, γ is body effect coefficient, VTO is the zero bias threshold voltage. The proposed DTMOS has a high threshold voltage at zero bias and low threshold voltage at Vgs = Vdd.

The threshold voltage equation is written for a long channel NMOS transistor where drain-induced barrier lowering (DIBL) effect is neglected. The DTMOS configuration does not require any additional processing steps fabrication and the gate and body of the transistor can be connected with metal contact as described in Silicon-On-Insulator (SOI) model [27]. DTMOS was proposed for obtaining excellent subthreshold characteristics at ultra-low Vdd [27–29]. Although PMOS transistors can be connected easily as DTMOS transistor, NMOS transistors require triple-well process which is very expensive processes to produce DTMOS transistor with their own wells. Only PMOS transistors have been used as a DTMOS in this study. Voltage headroom has been consumed over the NMOS transistors so overall performance of the proposed active device is limited. MOS transistor's drain current is given by below Eq. (2).

$$I_D = I_S\left(\frac{W}{L}\right)exp\left(q\frac{V_{GS}-V_{TH}}{nkT}\right)\left[1-exp\left(-q\frac{V_{DS}}{kT}\right)\right] \quad (2)$$

According to the equation high frequency applications and strong inversion operations are not possible using this circuit because the transistor will saturate in weak inversion when VDS $\geq$ 3kT/q [17]. Under some limitations, bulk-DTMOS technique can be applied to cheap standard CMOS fabrication process without additional processing steps. The transconductance gm is described by

$$g_m = q\frac{I_D}{nkT} \quad (3)$$

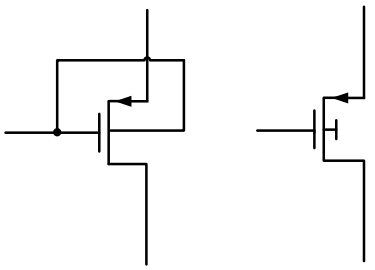

Figure 1. The schematic of DTMOS transistor and its widely used symbol [30].

The Block diagrammatic representation of proposed VDBA circuit symbol is shown in Figure 2. According to the figure p and n terminals are input, z and w terminals are output. The voltage difference is realizing with the differential-input OTA. Differential input voltage is transferred to the current at the terminal z by transconductance gain and the voltage drop at the terminal z is mirrored the terminal w which is the low impedance voltage output region. OTA, voltage controlled current source, has a high differential input stages and output stage. Electrical impedance transformation from one circuit to other is provided by buffered amplifier which is connected to the OTA's current output.

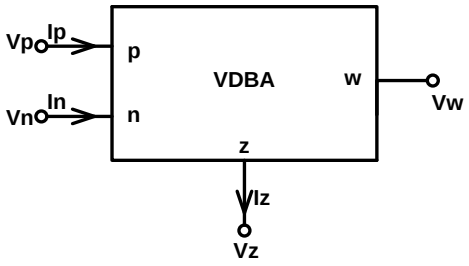

Figure 2. Block diagrammatic representation of VDBA.

The relation between terminal currents and voltages of the VDBA can be characterized by the following matrix:

$$\begin{bmatrix} I_p \\ I_n \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ g_m & -g_m & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_p \\ V_n \\ V_z \end{bmatrix} \quad (4)$$

Vp and Vn are the high-impedance voltage inputs, Iz is the high-impedance current output and Vw is the low-impedance voltage output can be noted by above matrix.

The internal construction of DTMOS based ULV and ULP proposed VDBA circuit is shown in Figure 3. This active device consists of an Operational Transconductance Amplifier (OTA) and a voltage buffer. The input stage of VDBA is composed of the differential-input OTA and the voltage buffer is connected to its current output. The transistors from M1 to M9 work as the OTA and the transistors from M10 to M16 work as the buffer amplifier.

The transistors from M1 to M5 and M11 to M13 are the PMOS DTMOS. DTMOS transistors, which have available voltage headroom, can be used efficiently under the ultra-low supply voltage of 0.4V [27–29].

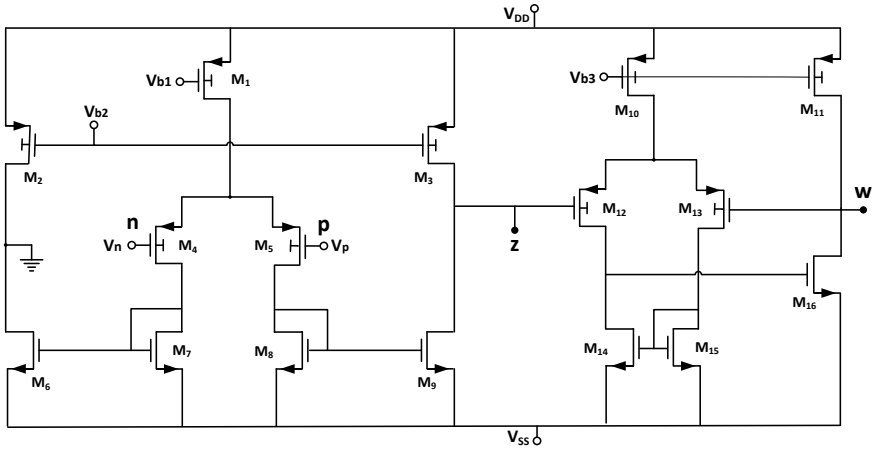

Figure 3. The proposed DTMOS-based VDBA circuit.

The circuits have been simulated by using LTSpice program with TSMC CMOS 0.18 µm process parameters. Table 1 shows the aspect ratios of the transistors for the proposed VDBA circuit. Supply Voltages are Vdd = -Vss = 0.2 V and all the biasing voltages are grounded in this application (Vb1 = Vb2 = Vb3 = 0 V).

Table 1. MOSFET dimensions used in VDBA simulations.

Transistor	Width	Length
M_1, M_2, M_3,M_{10}, M_{11}	5 µm	2 µm
M_4, M_5, M_{12}, M_{13}	300 µm	2 µm
M_7, M_8, M_{14}, M_{15}	50 µm	5 µm
M_6, M_9, M_{10}, M_{16}	100 µm	5 µm

The DC transfer characteristics of proposed VDBA input and output stages are shown in Figure 4 and Figure 5, respectively. The DC transfer characteristic of Iz against Vp for VDBA is shown in Figure 4 that is obtained when the terminal n which is the one of the input terminal is grounded. The DC transfer characteristics of Vz-Vw for the VDBA is shown in Figure 5. While the lower boundary of the voltage Vw for VDBA is determined as VWmin = 145 mV, the upper boundary of voltage Vw for VDBA is the positive supply voltage of the VDBA. It can be summarized that input voltage swing is between -145 mV to 200 mV under ±200 mV supply voltages. The AC transfer characteristics of input and output stages of proposed VDBA are shown in Figure 6 and Figure 7, respectively. The transconductance of proposed active circuit's gm is depicted in Figure 7 where it is found approximately 64 nA/V with a 3dB bandwidth of 3.66 kHz. The circuit performance of the proposed VDBA is summarized in Table 2.

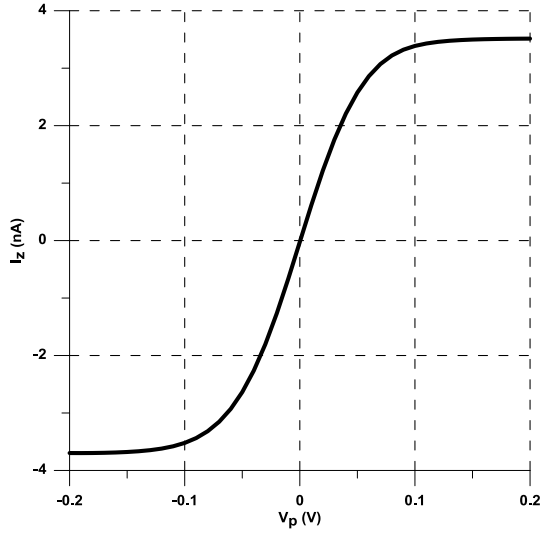

Figure 4. The DC characteristic of input stage of the proposed active device.

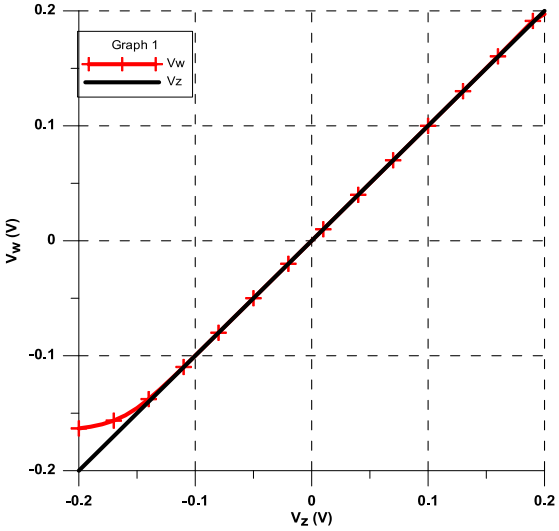

Figure 5. The DC characteristic of output stage of the proposed active device.

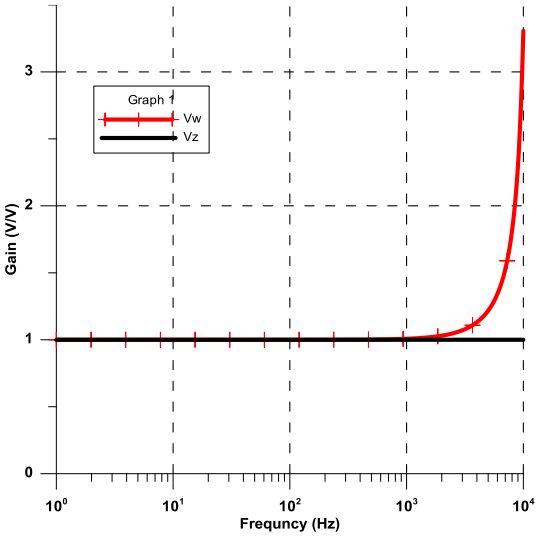

Figure 6. The AC characteristic of output stage of the proposed active device.

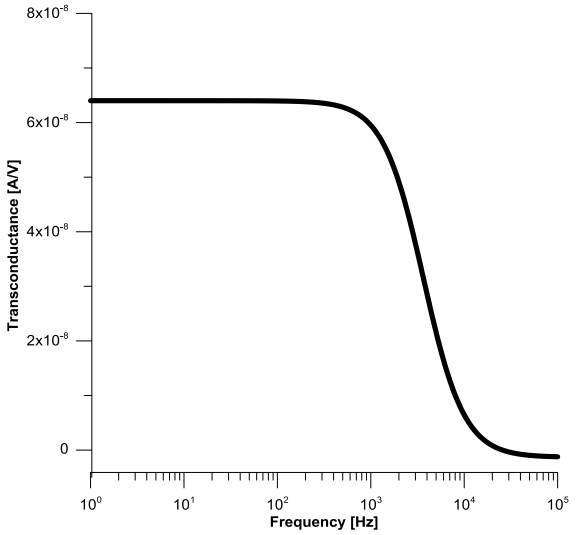

Figure 7. The transconductance of proposed active device.

Table 2. Performance summary of the proposed VDBA

Technology	0.18µm TSMC
Supply Voltage	±200 mV
Input Voltage Range	-145 mV - +200 mV
Power Consumption	6.22 nW
Transconductance	64 nA/V
Input Impedance (n terminal)	500 GΩ
Input Impedance (p terminal)	877 GΩ
Output Impedance (z terminal)	5.26 MΩ
Output Impedance (w terminal)	205

3. The Filter Application of Proposed VDBA

The performance of the proposed active element was analyzed with a biquad filter application. The voltage-mode filter is illustrated in Figure 8. The filter consists of two VDBA devices and two capacitors. The capacitance values of C1 and C2 are 100 pF. The transfer function can be expressed depending on the voltage status of V1 and V2. The filter is obtained different types of filter depending on voltage status of V1 and V2. The four filter functions are summarized in Table 3.

Figure 9 shows that responses of proposed VDBA based filters such as Low-Pass Filter (LPF), High-Pass Filter (HPF), Band-Pass Filter (BPF), and Band-Reject Filter (BRF).

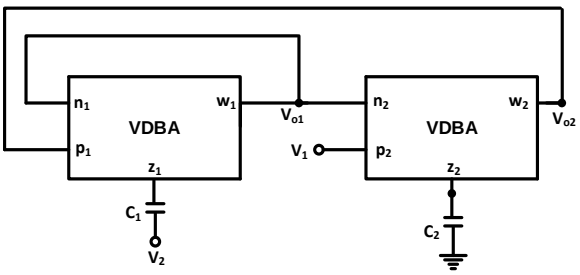

Figure 8. The voltage-mode filter configuration.

Table 3. The filter functions depending on the input and output status.

Input Voltage Status	Output Function
$V_1 = V_{in}$, $V_2=0$	$V_{o1}=\frac{V_1 g_{m1} g_{m2}}{s^2 C_1 C_2+s g_{m2} C_1+g_{m1} g_{m2}}$ (LPF)
$V_1 = 0$, $V_2= V_{in}$	$V_{o2}=\frac{V_2 g_{m2} s C_1}{s^2 C_1 C_2+s g_{m2} C_1+g_{m1} g_{m2}}$ (BPF)
$V_1 = 0$, $V_2= V_{in}$	$V_{o1}=\frac{V_2 s^2 C_1 C_2}{s^2 C_1 C_2+s g_{m2} C_1+g_{m1} g_{m2}}$ (HPF)
$V_1 = V_{in}$, $V_2= V_{in}$	$V_{o1}=\frac{V_1 g_{m1} g_{m2}+V_2 s^2 C_1 C_2}{s^2 C_1 C_2+s g_{m2} C_1+g_{m1} g_{m2}}$ (BRF)

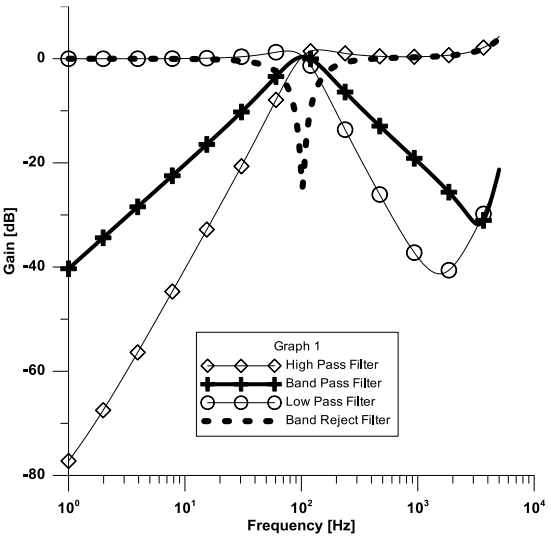

Figure 9. The simulation results of the proposed filter.

The pole frequency (ω_0) and the quality factor (Q) are given by Eq. (5) and Eq. (6), respectively, for all the responses;

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{5}$$

$$Q = \sqrt{\frac{g_{m1}C_2}{g_{m2}C_1}} \tag{6}$$

The passive sensitivities of the pole frequency (ω_0) and the quality factor (Q) for the proposed configuration with respect to active and passive elements yield;

$$S_{(g_{m1})}^{(\omega_0)} = S_{(g_{m2})}^{(\omega_0)} = -S_{(C_1)}^{(\omega_0)} = -S_{(C_2)}^{(\omega_0)} = \frac{1}{2} \tag{7}$$

$$S_{g_{m1}}^{Q} = -S_{g_{m2}}^{Q} = -S_{C_1}^{Q} = S_{C_2}^{Q} = \frac{1}{2} \tag{8}$$

It is clearly observed from Eq. (7) and Eq. (8) that passive and active sensitivities of pole frequency (ω_0) and quality factor (Q) for the proposed configuration do not exceed unity in magnitude. Temperature is an important factor for very low frequency filters with large time constants. The temperature has been changed from 0 °C to 75 °C and results are shown in Figure 10. Output total harmonic distortion (THD) values of the proposed filter at the 100 Hz frequency with respect to the input voltage are depicted in Figure 11. The total harmonic distortion of the filter obtained is less than 2% for inputs not exceeding 50 mV peak to peak voltages as shown in Figure 11. The obtained results show that the THD remains within acceptable limits.

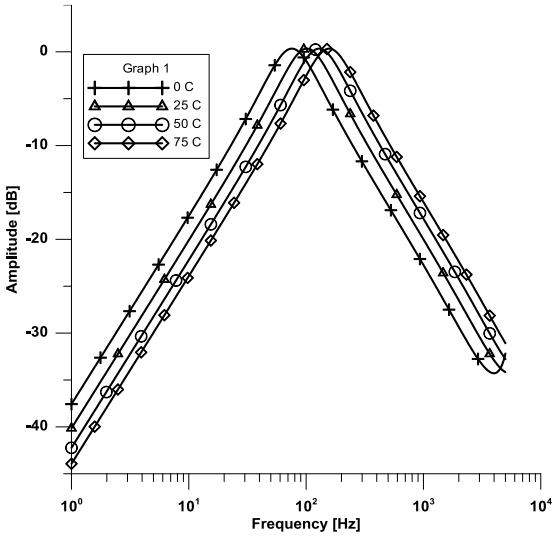

Figure 10. The change in the frequency depends on the temperature.

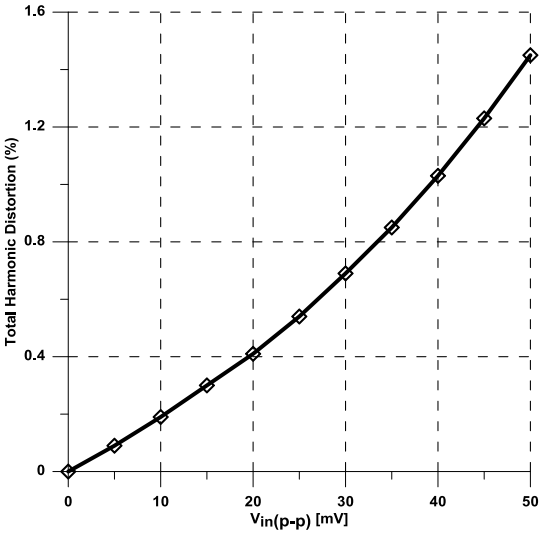

Figure 11. THD values of the proposed filter at the 100 Hz frequency.

5. Conclusions

In this study, DTMOS-based VDBA circuit was proposed. The proposed active circuit is able to work with 0.4 V voltage and only consuming 6.22 nW, which are suitable value for ultra-low voltage and ultra-low power operations. The proposed VDBA was tested with an application example of the filter. The LTSpice simulation results were depicted and according to simulations, both VDBA and filter have performed very well. Sensitivity analyses and percent of the total harmonic distortion has been found. The proposed active block has been worked in weak inversion area, so the working frequency is not very high. It works in low frequencies. It is believed that the proposed DTMOS based VDBA circuit and filter will be useful in the design of ULV and ULP analog signal processing applications and biomedical applications.

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