Research Article GU J Sci, Part A, 11(1): 235-244 (2024) 10.54287/gujsa.1405552

Gazi University
Journal of Science
PART A: ENGINEERING AND INNOVATION
http://dergipark.org.tr/gujsa

On the voltage dependent series resistance, interface traps, and conduction mechanisms in the Al/(Ti-doped DLC)/p-Si/Au Schottky Barrier Diodes (SBDs)

Sabreen A. HAMEED[1*] Öznur BERKÜN[2] Seçkin Altındal YERIŞKIN[3]

[1] *Department of Physics, College of Science, University of Diyala, Diyala, Iraq*
[2] *Department of Nanotechnology Engineering, Faculty of Sciences, Zonguldak Bulent Ecevit University, Zonguldak, Türkiye*
[3] *Vocational Highschool of Technical Sciences, Department of Chemistry and Chemical Processing Technologies, Gazi University, Türkiye*

Keywords

(Ti:DLC) interlayer Al/(Ti:DLC)/p-Si Schottky Diodes

Origin of series resistance and interface states

Conduction mechanisms

I-V, and C-V and G-V measurements

Abstract

In this study, Al-(Ti:DLC)-pSi/Au Schottky barrier diode (SBD) was manufactured instead of conventional metal / semiconductor (MS) with and without an interlayer and then several fundamental electrical-characteristics such as ideality factor (n), barrier height Φ_B series and shunt resistances (R_s, R_{sh}), concentration of acceptor atoms (NA), and width of depletion-layer (Wd) were derived from the forward-reverse bias current/voltage (I-V), capacitance and conductance as a function of voltage (C/G-V) data using various calculation-methods. Semi logarithmic IF-VF plot shows a linear behavior at lower-voltages and then departed from linearity as a result of the influence of series resistance/Rs and organic-interlayer. Three linear regions can be seen on the double-logarithmic IF-VF plot. with different slopes (1.28, 3.14, and 1.79) in regions with low, middle, and high forward bias, which are indicated that Ohmic-mechanism, trap-charge-limited-current (TCLC) mechanism, and space-charge-limited-current (SCLC) mechanism, respectively. Energy dependent surface states (Nss) vs (Ess-Ev) profile was also obtained from the Card-Rhoderick method by considering voltage-dependence of n and Φ_B and they were grown from the mid-gap energy up to the semiconductor's valance band (Ev). To see the impact of Rs for 1 MHz, the measured C/G-V graphs were amendment. All results are indicated that almost all electrical parameters and conduction mechanism are quite depending on R_s, N_{ss}, and calculation method due the voltage dependent of them.

Cite

Hameed, S. A, Berkün, Ö., & Yeriskin, S. A. (2024). On the voltage dependent series resistance, interface traps, and conduction mechanisms in the Al/(Ti-doped DLC)/p-Si/Au Schottky Barrier Diodes (SBDs). *GU J Sci, Part A, 11*(1), 235-244. doi:10.54287/gujsa.1405552

Author ID (ORCID Number)

0000-0002-1696-8705 Sabreen A. HAMEED
0000-0002-5854-9157 Öznur BERKÜN
0000-0002-9772-1212 Seçkin Altındal YERIŞKIN

Article Process

Submission Date 15.12.2023
Revision Date 23.01.2024
Accepted Date 08.03.2024
Published Date 25.03.2024

1. INTRODUCTION

The metal/semiconductor (MS) Schottky barrier diodes (SBDs) with and without an insulator-layer are main electronic devices due to their quick switching times, low-forward bias voltage operation, long lifetime and low capacitance (Card & Rhoderick, 1971; Sze & Ng, 2006; Cheung & Cheung, 1986; Nicollian & Brews, 1982; Reddy et al., 2022). In application, many sources may be affected on their performance like the formed a native or deposited interlayer on a semiconductor wafer's surface, its thickness and homogeneity, the availability of many interface traps or states at interlayer (semiconductor) interface and (R_s), barrier in-homogeneities at junction, fabrication processes, and electric field (Cheung & Cheung, 1986; Nicollian & Brews, 1982; Reddy et al., 2022; Ulusoy et al., 2023). The perfect case in structures of MS and MIS is diverged from by all of these sources. Among them, the most effective ones are the fabrication processes of them, the existence of high value of Rs, interface traps (N_{ss}), and the thickness and homogeneity of deposited interlayer at M/S interface, applied electric field (E=V/d), and the concentration of atoms injected into the semiconductor (Sharma & Tripathi, 2013).

*Corresponding Author, e-mail: sabreenalhameed19@gmail.com

It is thought that by using a high-dielectric interlayer, the efficiency of MS type SDs can be improved. For instance, the use such interlayer can be decreased leakage current, ideality factor, R_s, N_{ss} and maximize the rectification ratio ($RR=I_f/I_r$), barrier height (BH), shunt resistance (R_{sh}), respectively (Yerişkin et al., 2017; Berkün et al., 2023). As a result, over the past twenty years, several physicists, chemists and materials researchers have begun to use new interfacial layers like pure or polymers doped with metal or metal-oxide, DLC with or without metals, and some composites among semiconductor and metal to enhance the effectuation of MS type SDs (Berkün et al., 2023; Lin et al., 2013).

Diamond like carbon (DLC) thin film is a Amorphous carbon that is moderately stable (a:C) with $sp^2$and sp^3 bonds, or amorphous-carbon (a-C:H) which is including H atom in its structure and also it has high solidity, infrared energy transmittance, chemical stability, low thermal, large thermal conductivity and stellar characteristics like large electrical resistance. The Ti doped DLC has a great interlayer (35-100 nm) and excellent transparency (Berkün et al., 2023; Lin et al., 2013; Güçlü, 2023; Demirezen et al., 2022). Doping of DLC can be formed by metallic or non-metallic elements. Ti has a particular appeal among non-metals since it makes DLC more conductive and reduces the band gap. Therefore, in this study, Al-(Ti:DLC)pSi-Au (MIS) type SBDs were created instead of conventional MS SD with/without an insulator layer. Following that some of their important electrical variables were computed using various calculating methods by I-V and (C/G)-V graphs to determine how voltage-dependent they were.

2. MATERIAL AND METHOD

In this research, To create Al-(Ti: DLC)-pSi-Au SDs, the (Ti: DLC) inter-layer was formed onto Boron-doped (p-Si) single wafer by electrochemical deposition technique. Before the fabrication, wafer doped with B with <100> orientaion, ~300 μm thickness, 5.08 cm diameter, and 1–10 Ω.cm resistivity had been washed in an ultrasonic-bath using the RCA cleaning method in a solution of (18 M) deionized-water, HF, and (H_2O: HCl) solution. The wafer was then dried by N_2-gas before being processed into a 150 nm thick, at 10^{-7} Torr. The back-side of wafer was coated with Au by using thermal evaporation technique and then annealed at 500 ^oC to ensuring ohmic contact. After that (Ti:DLC) interlayer was grown onto wafer utilizing electrochemical-deposition method. Finally, 150nm thick and 1mm diameter high-pure (99.999%) Al Schottky contacts were coated on the (Ti:DLC) interlayer at 10^{-7} Torr. The IV and (C/G) – V of the sample have been measured utilizing Keithley – 2400 I-V source meter and HP 4192 A impedance analyzer, respectively. For more information on the fabricated processes, prepared (Ti:DLC), and structural analysis can find in our previous study (Berkün et al., 2023).

3. RESULTS AND DISCUSSION

3.1. Forward/reverse bias iv characteristics

Al/(Ti:DLC)/p-Si/Au SD produced at room temperature (RT) forward bias $\ln(I_f)$-V_f plot is shown in Figure 1. It is clear that this curve has good rectifier-behavior and linear-part between 0.04 V and 0.25 V and then deviated from linearity due to (Ti:DLC) interlayer and R_s effects (Card & Rhoderick, 1971; Sze & Ng, 2006). The conventional thermionic emission (TE) theory is usually used in MS/MIS type SDs to study the CM and calculation electrical-parameters. Based on TE theory, the current-voltage relation in the SDs with R_s and higher value of n could be described as follows (Card & Rhoderick, 1971; Sze & Ng, 2006; Cheung & Cheung, 1986).

$$I = (AA^*T^2).\exp\left(-\frac{q\Phi_{B0}}{kT}\right)[\exp(q(V\text{-}IR_s)/nkT)\text{-}1)] = I_o\left[\exp\left(\frac{q}{nkT}(V - IR_s) - 1\right)\right] \quad (1)$$

Here; k, T, IRs, and I_o or Is are the Boltzmann-constant, temperature (K), voltage drops SD, and saturation-current. Based on TE theory, the values of I_o, n, Φ_{Bo} have been calculated from the intercept and slope of $\ln(I_f)$-V_f plot as $1.71x10^{-7}$A, 1.98, 0.64 eV, respectively.

$$n = \frac{q}{kT}\left(\frac{d(V)}{d(\ln(I))}\right) \quad (2a)$$

$$\Phi_{Bo} = \frac{kT}{q} \, Ln\left(\frac{AA^* \, T^2}{I_o}\right) \tag{2b}$$

The biggest value of n is the result of presence of N_{ss}, Interlayer, its thickness, and barrier inhomogeneity's (Card & Rhoderick, 1971; Sze & Ng, 2006; Cheung & Cheung, 1986), but the non-saturated reverse current was attributed to image-force reducing BH, and generation-recombination (Card & Rhoderick, 1971; Sze & Ng, 2006).

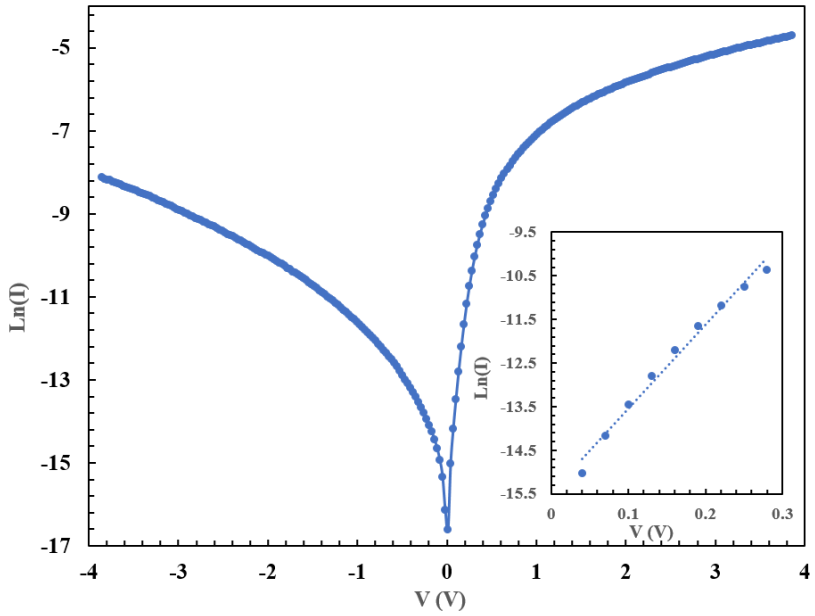

Figure 1. *The Ln(I)– V curve of the Al-(Ti:DLC)-pSi-Au SBD*

The voltage-dependent resistance (R_i) of the Al-(Ti:DLC)-pSi-Au SBD was calculated with Ohm–Law and depicted in Figure 2.

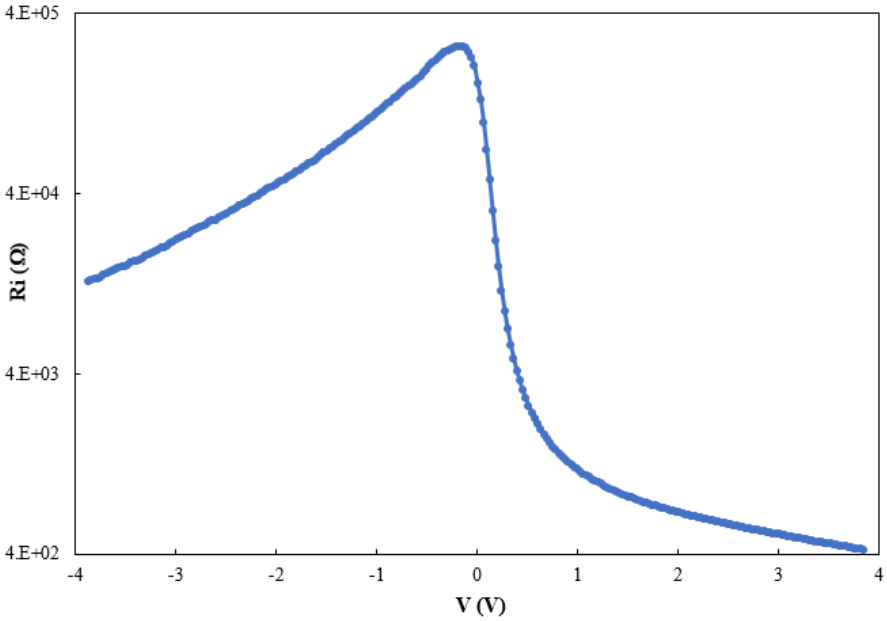

Figure 2. *The (Ri)- V curve of the Al/(Ti:DLC)/P-Si/Au SBD*

Figure 2 illustrates, the R_i beginning as almost constant both the higher forward and reverse voltages, and so corresponds actual values of R_s (=407Ω) and R_{sh} (=11800Ω). To see the voltage/method dependent of them (n, Φ_{Bo}, and R_s), they were also calculated from Cheung's functions and it allow us to calculate in the

descending curve of the ln(I_f)-V_f plot at moderate- forward-voltages given in Eq. 2(a) and (b). As shown in Figure 3, both dV/dln(I) and H(I) versus V curves have excellent linear in large range of current/voltage (Cheung & Cheung, 1986).

$$\frac{dV}{dln(I)} = \frac{nkT}{q} + R_s I \tag{3a}$$

$$H(I) = V - \frac{nkT}{q}.\mathrm{Ln}\left[\frac{I}{T^2 A^* A}\right] = R_s I + \Phi_{B0} n \tag{3b}$$

From Eq. 3(a), the intercept voltage and slope (Figure 3) is given the nkT/q and Rs. The intercept and slope of the Eq. 3(b) by using the n value (=intercept/(kT/q)) is also given the $n\Phi_B$ and R_s as directly. Thus, R_s and n were determined as 324 Ω and 12.65 from Eq-3(a) and Rs and Φ_B are 293Ω and 0.486eV, respectively. The voltage dependence and calculation method lead to some discrepancies between TE and Cheng Functions. Because, whereas the TE theory is valid at moderate forward-voltages. Cheung functions are valid at high forward voltages.

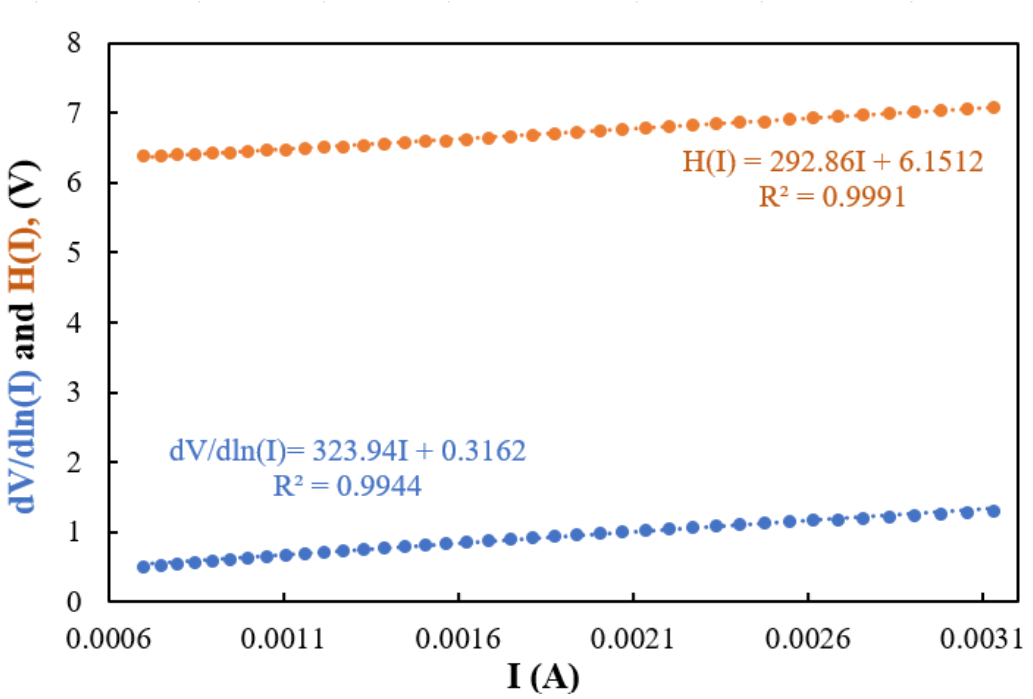

***Figure 3**. The dV/dln(I) − I and H(I)−I curves of the Al-(Ti:DLC)-pSi-Au SBD*

To calculate the possible conduction mechanisms (CMs) in region of I_f-V_f graphic with a double-logarithmic scale were drawn in the forward bias regime (Figure 4). In this Figure *Ln(I_F)–Ln(V_F)* curev of the SBD has three linear-regions with unlike slopes because of the present changes in the form $I \propto V^m$(Sze & Ng, 2006; Sharma & Tripathi, 2013; Demirezen et al., 2022). which are associate to low, inter-mediate in addition to at enough high voltages. The slope of them were found as 1.279, 3.141, and 1.796, respectively and so we can say that in lower-voltages Ohmic-behavior, in moderate-voltages, trap-charge limited current (TCLC), at high forward voltages, space-charge limited current (SCLC) are dominate CMs, respectively. Because, Ohm's law appears to be effective in first-region, with slope closes ~1. The TCLC is effective when slope higher than 2, and SCLC is effective when the slope is closer ~2.

Each of the existence of N_{ss} between interlayer and semiconductor interface is too more influential on the moderate voltages I-V properties and they often formed when the surface periodic lattice was interrupted, preparation for cleaning and manufacturing, doping donor/acceptor atoms, impurities and other organic contaminations in laboratory environment. Based on Card-Rhoderick (Card & Rhoderick, 1971; Sze & Ng, 2006), n value becomes more than unity for SDs with N_{ss} that is equivalent to semiconductor (if inter-layer is more than a few nm), and is given as follow:

$$n(V) = \frac{q}{kT}\frac{dV}{dln(I)} = 1 + \frac{d_i}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \quad (4a)$$

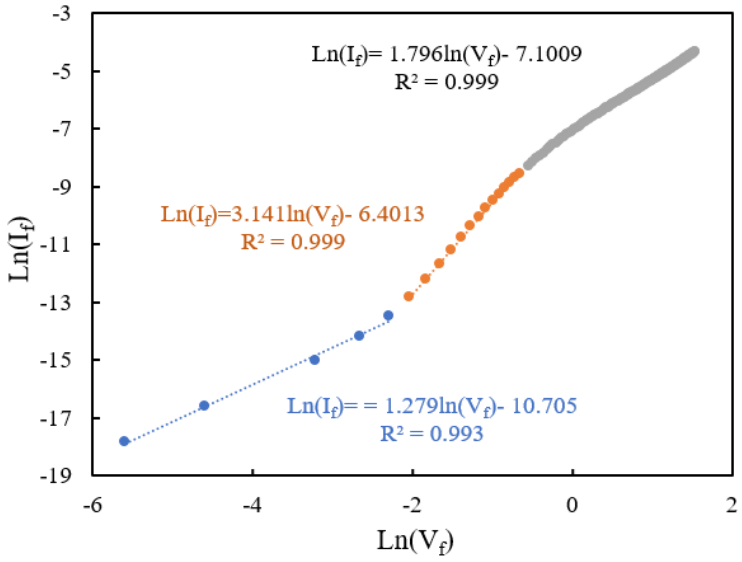

Figure 4. *The Ln(I_F) and Ln(V_F) curves of the Al-(Ti:DLC)-pSi-Au SBD*

Here, the values of ε_i / ε_s, W_D, and d_i are the dielectric permittivity of the inter-layer and semiconductor, width of the depletion layer, the inter-layer thickness, respectively. The magnitude of εi and ε_s was taken as $113\varepsilon_o$ and $11.8\varepsilon_o$. Here, (ε_o = permittivity of vacuum). As a result, the energy-dependent N_{ss} profile in relation towards the highest region of the valance-band (Ev) is as below. (Card and Rhoderick, 1971; Sze & Ng, 2006).

$$E_{ss} - E_v = q(\Phi_e - V) \quad (4b)$$

In Eq.4, $\Phi_e(V)$; V-dependence BH. The N_{ss}- (E_{ss}-E_v) plot was obtained by using following relation suggested by Card-Rhoderick (Card & Rhoderick, 1971) is shown in Figure 5.

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \quad (4c)$$

From Figure 5, the N_{ss} increases at about from mid bandgap of semiconductor (~Eg/2) towards top of E_v as exponentially which means they range from $6.42x10^{12}$/(eVcm^2) at (0.6263-E_{ss}) eV to $5.92x10^{13}$/(eVcm^2) at (0.385-E_{ss}) eV which are suitable for MIS type SBD.

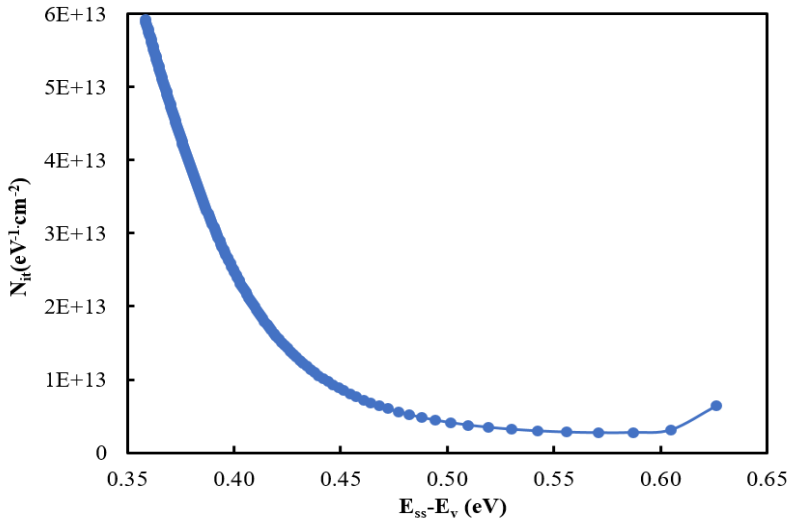

Figure 5. *The Nss- (Ess-Ev) curve of the Al-(Ti:DLC)-pSi-Au SBD*

3.2. Forward & reverse bias c/g-v characteristics

Figure 6 shows the C-V and G/ω-V graphs of the Al-(Ti:DLC)-pSi-Au SBD. As depicted in Figure 6, these two-plots have accumulation, depletion, and inversion regimes such as metal/oxide/semiconductor (MOS) structure. But, the (G/ω-V) plot, exhibits a distinctive peak at ~0.8 V as a result of a special arrangement of N_{ss} between (Ti:DLC)/P-Si interface (Sze & Ng, 2006; Cheung & Cheung, 1986). The R_s has also increased effectiveness on each of the C-V and G/ω-V curves like I-V at enough high positive voltages. R_s value are usually derived from the back and Schottky contacts, the cables used for the probe from rectifier contact, the semiconductor bulk-resistivity, and in-homogeneities of the doping concentration atoms (Sze & Ng, 2006; Cheung & Cheung, 1986; Nicollian & Brews, 1982; Reddy et al., 2022). But, N_{ss} are usually originated from are interruption in the periodic lattice of the semiconductor-surface, cleaning, fabrication-processes, and some contaminates in the bulk semiconductor, within the confines of a laboratory (Sze & Ng, 2006; Cheung & Cheung, 1986; Reddy et al., 2022; Ulusoy et al., 2023; Sharma & Tripathi, 2013).

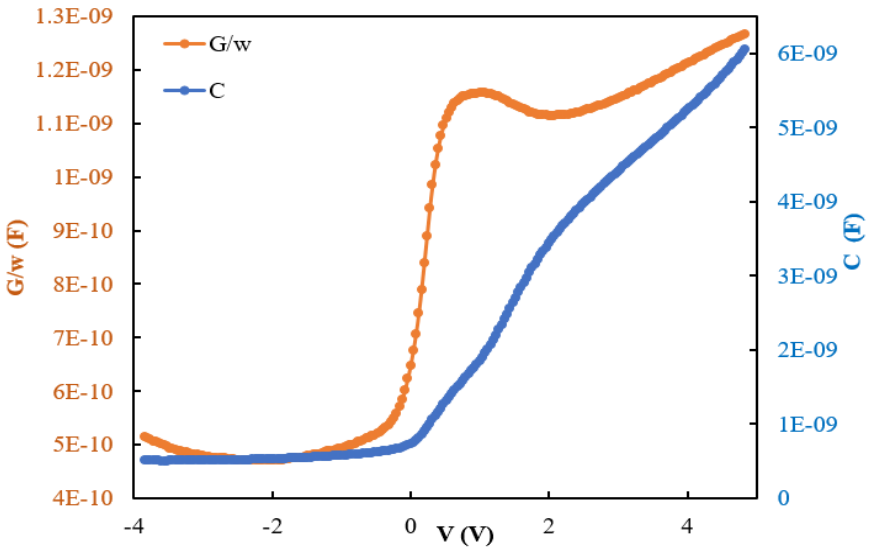

Figure 6. *The C-V and G/ω-V curves of the Al-(Ti:DLC)-pSi-Au SBD*

In order to investigate the voltage dependent resistance (R_i) on the *C–V* and *G/ω–V* graphs of Al-(Ti:DLC)-Psi-Au SBD, it was derived from these values by using Nicollian-Brews technique by applying the following relation which is presented in Figure 7. (Nicollian & Brews, 1982).

$$R_i\,(V) = G_{mi}/[(G_{mi}^2+(\omega C_{mi})^2)] \quad (5)$$

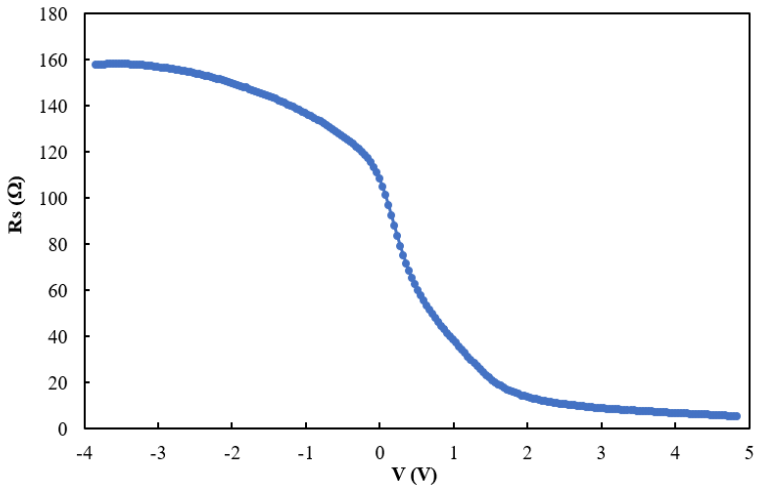

Figure 7*. The R_s – V plot of the Al-(Ti:DLC)-pSi-Au SBD*

In Eq.5, C_{mi} is the capacitance, G_{mi} is the conductance which calculated for a bias voltage, ω refers to angular frequency and it's equal to (2πf). As depicted in Figure 7, the Ri quantity reduces with increasing voltage before reaching a nearly constant value (5.29) at accumulation regime which is identical to the actual value of Rs. This is considerably suitable for MIS type SBD. The effect of Rs can be minimized when The impedance-measurements carried out at low frequency or adjustable of them at sufficient frequencies (f≥500 kHz) to eliminate Rs influence on them. To view the Rs influence on this high frequency C–V and G–V graphs of the Al-(Ti: DLC)-Psi-Au SBD, they fixed by utilizing the value of Rs as given next relations and then both the measured and corrected Cc/V and Gc/V plots are presents in the Figure 8 a) and b), respectively (Sze & Ng, 2006; Cheung & Cheung, 1986).

$$C_c = \frac{[G_{ma}^2+(\omega C_{ma})^2]C_{ma}}{a^2+(\omega C_{ma})^2} \quad (6a)$$

$$G_c = \frac{[G_{ma}^2+(\omega C_{ma})^2]a}{a^2+(\omega C_{ma})^2} \quad (6b)$$

In Eqs-6(a, b); $(a = G_{ma} - [G_{ma}^2 + (\omega C_{ma})^2]R_s)$ is a correction-coefficient. When the corrected plots were represented in Figure 8 and Figure 9. When these fixed Cc-V and Gc/-V plots compared the calculated C_m–V and G_m/ω–V plots (Figure 8); there is an important discrepancy between of them in reverse-bias region, but the Cc starts to increase both in depletion and accumulation region. While G_c/ω–V plot has a recognizable peak at 0.8V. Therefore, we show that Rs especially is more efficient at accumulation-region, while N_{ss} are efficient in depletion-region. Recently, similar findings for MIS type structures have been also documented in the literature (Sze & Ng, 2006; Nicollian & Brews, 1982; Demirezen et al., 2022).

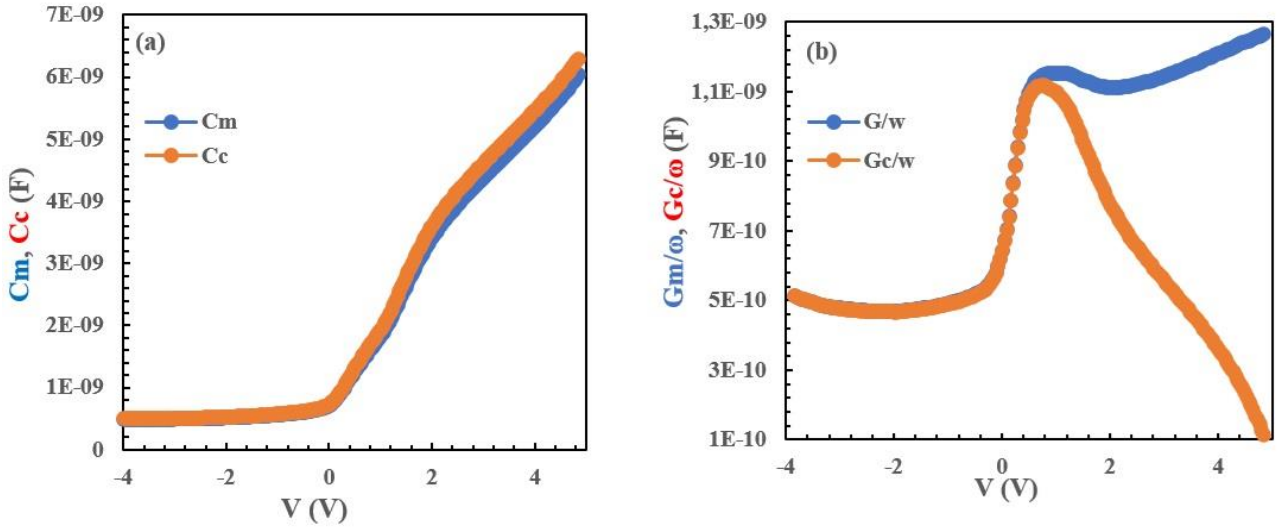

Figure 8. *a) The C_m-V and Cc-V, b) G_m/ω-V and Gc/ω-V curves of the Al-(Ti:DLC)-pSi-Au SBD at 1MHz*

The depletion-layer capacitance (C) for MIS type SBDs is given as follows (Sze & Ng, 2006).

$$C = \frac{|\partial Q_{SC}|}{\partial V} = \sqrt{\frac{q\varepsilon_s\varepsilon_0 N_A}{2\left(V_o - V - \frac{kT}{q}\right)}} \quad (7a)$$

Eq. 7(a) can be arranged as follows for the extraction of fundamental electrical characteristics of the MIS-structures in the region of reverse bias as given follow.

$$C^{-2} = \frac{2\left(V_o - Vr - \frac{kT}{q}\right)}{q\varepsilon_s\varepsilon_0 N_A} \quad (7b)$$

Here, V_o is intercept-voltage of (C^{-2}-V) graph, the V_D value (diffusion potential) is obtained from ($V_D = V_o + kT/q$). The total number of N_A was extracted from the slope of C^{-2}-V curve (Figure 9):

$$N_A = \frac{2}{q\varepsilon_s\varepsilon_o A^2\left(\frac{dC^{-2}}{dV}\right)} \quad (7c)$$

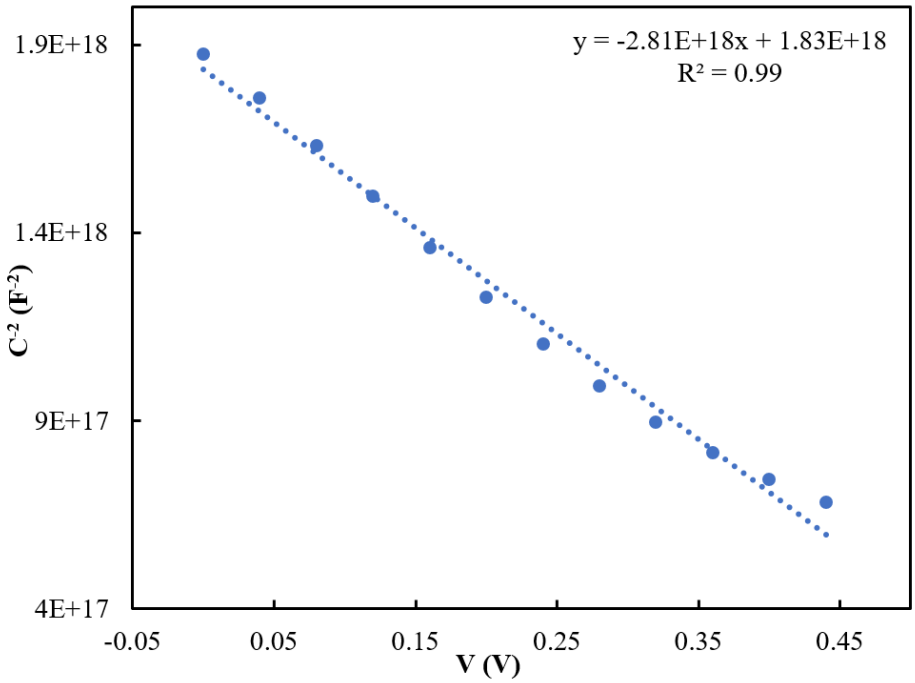

Figure 9. *The C^{-2} - V curves of the of the Al-(Ti:DLC)-pSi-Au structure SBD*

Following relations used to calculate some basic electrical parameters such W_D, E_F, and Φ_B (CV), this values obtained through the use of intercept-voltage (Vo) and ($1/C^2$-V) slope, respectively (Sze & Ng, 2006; Reddy et al., 2022).

$$W_D = \sqrt{\frac{2\varepsilon_s\varepsilon_0 V_o}{qN_D}}\ , \qquad E_F = \left(\frac{kT}{q}\right) Ln\left(\frac{N_c}{N_D}\right) \qquad \text{and} \quad \Phi_{B(CV)} = V_o + \frac{kT}{q} + E_F \quad (8)$$

Thus, the V_o, N_A, W_D, E_F and Φ_B(CV) values were calculated as 0.651 V, $6.90x10^{16}$ cm^{-3}, $11.10x10^{-6}$cm, 0.133 eV, and 0.89 eV, respectively. Estimated amount of BH from the intercept of C^{-2}-V plot (Φ_B(CV)=0.89 eV is lower than that observed from forward bias plot ln(I)-V plot (Φ_{Bo}(IV)=0.64 eV) at about the value of E_F. The Φ_B(CV) and (Φ_{Bo}(IV)) differences related to the nature of measuring systems which are associated to forward & reverse voltages. That is the apparent BH from the semiconductor to the metal is always at about E_F smaller than the BH they from the metal to the semiconductor. Recently, some basic electrical parameters of the MIS type SBD_S were obtained from TE theory and Cheung functions by various researchers as given in the Table 1. The observed some discrepancies between these parameters are the result of different calculated method and voltage dependent of them. On the other hand, the observed higher value of n can be explained by the existence of interlayer and surface states, doping concentration of acceptor atoms, and barrier inhomogeneity.

4. CONCLUSION

Within this study, Al-(Ti: DLC)-pSi-Au (SD) was fabricated instead of normal MS and MIS type SDs and then it's some main electrical-parameters n, Φ_B, R_s, R_{sh}, N_a, and W_d which has been derived from the I-V and C/G-V measurements by various calculation- techniques. The I_F-V plot shows good linear behavior at lower voltages and then deviated linear case due to effect of Rs and polymer/organic interlayer. On the other hand, ln(I_F)-ln(V_F) plot shows three different linear regions with different-slopes (1.28, 3.14, and 1.79) at low, intermediate and high bias voltages. These regions are corresponding to the Ohmic, TCLC, and SCLC, respectively. Energy dependent profile of N_{ss} located between (Ti: DLC) and p-Si was extracted by using the Card-Roderick method by taken into account voltage dependence of n and Φ_B and they were grown from the midgap towards the top of Ev of semiconductor. Voltage-dependent profile of Ri is also determined by Ohm-Law and Nicollian-Brews method to observe the impact of Rs on the I–V and C/G–V characteristics at 1 MHz. Several important electrical-characteristics like n, Φ_B, and Rs values were derived from forward bias I-V

measurements with using theory of TE and Cheung-functions show some inconsistency as a result of the calculating procedure and voltage-dependent of them. The Φ_B value resultant from the C^{-2}-V graphs is larger than the forward I-V measurements as nearly Fermi level (E_F) is also a result measured method. All findings indicate that the created Al-(Ti:DLC)-pSi-Au (SD) may successfully replace traditional MS or MIS type SDs in terms of economical in cost, flexibility, and easy grown method without more energy consumption.

Table 1. *Some basic electrical parameters of the Al-(Ti:DLC)-pSi/Au SBD obtained from various methods.*

Symbol	This work	Zeyrek,S. (2015)	Güçlü, Ç.Ş. (2023)	Doğan,H. (2022)	Yerişkin, S.A., et al. (2017)
n	1.89 (TE) 12.6 (Cheung)	6.17 (TE) 6.91 (Cheung)	2.348	1.27	1.464
Φ_{Bo} (eV)	0.64 (TE) 0.486 (Cheung)	0.714 (TE) 0.66 (Cheung)	0.576	0.82	0.790
R_s (□)	407 (TE) 308.5 (Cheung)	448.5 (Cheung)	-	9.3 (Cheung)	530
R_{sh} (M□)	0.0118	-	-	-	512
w_d (cm)	$11.1x10^{-6}$	-	-	-	-

ACKNOWLEDGEMENT

This study was supported by TUBITAK with the research project number 121C396 and 121C458.

AUTHOR CONTRIBUTIONS

In this article, the contributions of the authors are equal.

CONFLICT OF INTEREST

The author declare no conflict of interest.

REFERENCES

Berkün, Ö., Ulusoy, M., Altındal, Ş., & Avar, B. (2023). On frequency and voltage dependent physical characteristics and interface states characterization of the metal semiconductor (MS) structures with (Ti:DLC) interlayer. *Physica B: Condensed Matter*, 666, 415099. https://doi.org/ 10.1016/j.physb.2023.415099

Card, H. C., & Rhoderick, E. H. (1971). Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes. Journal of Physics D: *Applied Physics*, 4(10), 1589-1601. https://doi.org/ 10.1088/0022-3727/4/10/319/meta

Cheung, S. K., & Cheung, N.W. (1986). Extraction of Schottky diode parameters from forward current-voltage characteristics. *Applied physics letters*, 49(2), 85–87. http://dx.doi.org/10.1063/1.97359

Demirezen, S., Altındal, Ş., Kalandaragh Y. A, & Akbaş, A. M. (2022). A comparison of Au/n-Si Schottky diodes (SDs) with/without a nanographite (NG) interfacial layer by considering interlayer, surface states (Nss) and series resistance (Rs) effects. *Physica Scripta*, 97(5), 055811. https://doi.org/ 10.1088/1402-4896/ac645f

Dogan, H. (2022). Parameter estimation of aı/p-si schottky barrier diode using different meta-heuristic optimization techniques. *Symmetry*, 14(11), 2389. https://doi.org/ 10.3390/sym14112389

Güçlü, Ç. Ş. (2023). A Comparison Electronic Specifications of the MS & MPS type Schottky Diodes (SDs) via Utilizing Voltage-Current (V-I) Characteristics. *Gazi University Journal of Science Part A: Engineering and Innovation*, 10, 62-69. https://doi.org/ 10.54287/gujsa.1212696

Lin, Y., Weng, C., Lin, Y., Shiesh, C., & Chen, F. (2013). Effect of C content and calcination temperature on the photocatalytic activity of C doped TiO_2 catalyst. *Separation and Purification Technology*, 116, 114 –123. https://doi.org/10.1016/j.seppur.2013.05.018

Nicolian, E. H., & Brews, J. R. (1982). Metal oxide semiconductor MOS physics and technology. *A Wiley Interscience Publication*, 495-502.

Reddy, N. N. K., Vattikuti, S. V. P., Verma, V. K., Singh, V. R., Alhammadi, S., Kummara,V.K., Manjunath, V., Dhanalakshmi, M., & Reddy,V. R. M. (2022). Highly sensitive and cost-effective metal-semiconductor-metal asymmetric type Schottky metallization based ultraviolet photodetecting sensors fabricated on n-type GaN. *Materials Science in Semiconductor Processing*, 138, 106297. https://doi.org/10.1016/j.mssp.2021.106297

Sharma. M., & Tripathi, S. K. (2013). Analysis of interface states and series resistance for Al/PVA:n-CdS nanocomposite metal–semiconductor and metal–insulator–semiconductor diode structures. *Applied Physics A*, 113, 491-499. https://doi.org/10.1007/s00339-013-7552-3

Sze, S. M., & Ng, K. K. (2006). Physics of Semiconductor Devices. New York, John Wiley & Sons, Inc.

Ulusoy, M., Badali,Y., Pirgholi Givi, G., Azizian Kalandaragh,Y., & Altındal, Ş. (2023). The capacitance/conductance and surface state intensity characteristics of the Schottky structures with ruthenium dioxide-doped organic polymer interface. *Synthetic Metals*, 292, 11343. https://doi.org/ 10.1016/j.synthmet.2022.117243

Yerişkin, S. A., Balbaşı, M., & Orak, İ. (2017). The effects of (graphene doped-PVA) interlayer on the determinative electrical parameters of the Au/n-Si (MS) structures at room temperature. *Journal of Materials Science: Materials in Electronics*, 28, 14040–14048. https://doi.org/ 10.1007/s10854-017-7255-1

Zeyrek, S. (2015).The effect of interface states and series resistance on current-voltage characteristics in (MIS) Schottky Diodes. *Afyon Kocatepe University Journal of Science & Engineering*, 15(2), 021101, 1-9. https://doi.org/ 10.5578/fmbd.9657