CHAOS
Theory and Applications
in Applied Sciences and Engineering

e-ISSN: 2687-4539
RESEARCH ARTICLE
Vol.6 / No.4 / 2024 / pp.249-256
https://doi.org/10.51537/chaos.1466919

Performance Evaluation of FPGA-Based Design of Modified Chua Oscillator

Muhammed Furkan Taşdemir [*β,1], **Anna Litvinenko** [α,2], **İsmail Koyuncu** [β,3] **and Filips Capligins** [α,4]

[*]SpacESPro Lab – Space Electronics and Signal Processing Laboratory, Riga Technical University, Riga, Latvia, [α]Institute of Radioelectronics, Riga Technical University, Riga, Latvia, [β]Department of Electrical Electronics Engineering, Faculty of Technology, Afyon Kocatepe University, Afyon, Türkiye.

ABSTRACT The chaotic systems are among the most important areas that have increased in popularity and are actively used in several fields. One of the most essential components in chaotic systems is the chaotic oscillator which generates chaotic signals. IQ-Math and floating point number systems are preferred number standards. In this study, the Modified Chua chaotic oscillator has been designed to work on FPGA chips using fixed point and floating point number representations, and both system version performances are compared. Euler numeric algorithm has been used to design the Modified Chua chaotic oscillator. In the first section of the study, the Modified Chua chaotic system based on fixed point has been composed the model in the Matlab Simulink and converted to VHDL with the help of Matlab HDL Coder Toolbox. In the second section of the study, the Modified Chua chaotic oscillator has been designed with VHDL based on floating point. Modified Chua chaotic oscillators which are composed with two different number standards have been tested using Xilinx ISE Design Tools in VHDL. Modified Chua chaotic oscillators which have two different number standards and designed, are synthesized for Virtex-6 on ML605 FPGA development board using Xilinx ISE Design Tools 14.2 program. The values that are achieved from the process of synthesizing and the process of maximum operating frequency have been presented. As a result, the study has found that fixed-point representation achieved a maximum operating frequency of 50.242 MHz, while the floating-point representation achieved 273.631 MHz.

KEYWORDS
Chaotic oscillators
Euler algorithm
FPGA chips
VHDL

INTRODUCTION

Nonlinear systems are structures where space nonlinearity and linearity exist only within certain limits. Behaviors that seem simple or trivial in a nonlinear system can lead to unpredictable changes and results. Chaotic systems are among the most actively used and researched areas within this broad spectrum. In recent years, chaotic systems have played an important role in solving increasing security problems worldwide. Economic and technological developments have led to an increase in the speed and capacity of information, which has, in turn, caused security problems. While massive amounts of information are transmitted without loss, each piece of information needs to be stored and encrypted according to the area in which it is used. In this context, the use of chaotic systems and the renewed focus on these systems created by chaotic fluctuations present promising approaches for solving these problems. Chaotic systems do not work as periodical systems, so the next results cannot be predicted (Litvinenko 2017a). Chaotic systems produce new values at each step, giving different results from previous values and generating unique subsequent values from earlier values. Chaotic systems are actively used in such areas as cybersecurity (Amir Anees 2018), voice and image processing (Fatih Özkaynak 2013; Mohamed L. Barakat 2013; Gabr 2023), optimization algorithms (Erkan Tanyıldızı 2017), the defense industry (Vasyuta *et al.* 2019), biomedical applications (Zhengxing Huang 2014), and mechatronics (Jorge Pomares 2014).

A study conducted by Linsheng Zhang et al. developed an automated system that transitions from a floating-point number system to a fixed-point number system based on Extreme Value Theory (Linsheng Zhang 2009). Babajans et al. achieved synchronization between two chaotic systems using the Vilnius chaotic oscillator, with results shared by researchers (Ruslans Babajans 2020). Litvinenko's research thesis illustrates the usage of generated chaotic systems such as logistic map, Bernoulli map, and tent map for DS-CDMA (Direct-Sequence Code Division Multiple Access) systems (Litvinenko 2017b). In another study, Litvinenko et al. proposed Chaos Shift Keying (CSK) based on the Modified

Manuscript received: 10 May 2024,
Revised: 11 October 2024,
Accepted: 31 October 2024.

[1]furkantasdemir123@gmail.com (**Corresponding author**).
[2]anna.litvinenko@rtu.lv
[3]ismailkoyuncu@aku.edu.tr
[4]filips.capligins@rtu.lv

Chua chaotic system, achieving synchronization between a transmitter and two receivers for data transmission (Litvinenko and A. 2019). Additional work by M. K. Gabr implemented an encryption and decryption system that employs the Chua circuit as one of the chaos generators (Gabr 2023). Arpaci's thesis introduced video encryption and decryption systems using a Modified Chua chaotic circuit for enhanced data transmission security (Arpaci 2019).

The daily pace of humanity has increased with the development of technology. When comparing the last decade's technological acceleration with that of the last 20 years, even though the time span is only twice as long, technological development has more than doubled. One important technology for meeting ever-growing humanity's needs, whether in academia or industry, is the FPGA (Field Programmable Gate Array). Nowadays, the active use of FPGA chips is crucial for digital system design. FPGA chips, which allow fast prototyping, parallel signal processing, and high working frequency capabilities in a whole-circuit structure, are preferred in resourceful signal processing tasks, such as chaotic system applications. FPGA chips have been extensively used in signal processing and real-time applications that require high performance with high processing power due to their significant advantages such as pipelined processing, low cost, re-programmability, and high throughput. FPGA chips are actively used in both academia and industry in fuzzy logic (Fatih Karataş 2020), image processing (Koyuncu 2022; Taşdemir 2020), biomedical systems (Fatih Karataş 2021), artificial neural networks (Murat Alcin 2016), and communication systems (Filips Capligins 2021).

FPGA, ASIC (Application Specific Integrated Circuit), and DSP (Digital Signal Processor) chips are preferred structures due to their high-frequency parallelism and special capabilities. These chips are generally differentiated from each other based on their production purpose and cost. While FPGA chips stand out with their re-programmability and flexibility, ASICs are more cost-effective than FPGA and DSP chips when produced in large quantities, but they do not have re-programmability features. As a result, they are industrially preferred over other chips. DSP chips excel in signal processing for more specialized areas such as image and sound processing. In one study, a stable modified fourth-order autonomous Chua chaotic system was developed using the Virtex 6 FPGA chip, achieving a frequency of 180.180 MHz with the RK4 (Fourth-order Runge-Kutta) numerical integration algorithm based on 32-bit IQ-Math floating-point numbers (Fei Yu 2020). In another study, Capligins et al. programmed an FPGA chip using a Modified Chua chaos generator for high-security networks and wireless communication methods (Filips Capligins 2021).

In this study, unlike classical number base studies, the performance analysis of two number bases has been performed. To ensure fair conditions and make the performance analysis more efficient, the comparison was made with a single-type chaotic system produced with two different number bases. A Modified Chua chaotic system was generated with both fixed-point and floating-point number bases. This approach reduces the impact of external factors when analyzing performance and equalizes conditions between both representations. This study provides an analysis of the importance of the materials to be used when designing a chaotic oscillator and how these materials should be selected, such as memory, experience, and cost requirements. Conversely, it provides guidance on how to produce the most effective chaotic oscillator with readily available materials.

The chip statistics, including comparison results with different studies related to Xilinx (AMD) and Altera (Intel) FPGA chips, are given in Table 1. This table includes critical parameters, such as maximum operating frequencies and numerical methods regarding fixed-point and floating-point number systems based on Lu-Chen, Lorenz, Liu, Chen, Chua; the Modified Chua used in this article, and CO and HO from the literature.

As a result of the study, the fixed point number-based chaotic oscillator provides less memory usage than the results that shared in the literature, while the floating point number-based oscillator provides clearer and more accurate results. These results explain the importance of chaotic oscillators considering the importance of past and present communication systems. In the second part of the study, general information about fixed and floating point number systems, Modified Chua chaotic oscillator and FPGA-based Modified Chua chaotic system is given. In the Third Section, 32-bit fixed point and floating point-based Modified Chua chaotic oscillator unit designs on FPGA chip and chip statistics obtained from the designs are presented. In the last section, the results obtained from the studies are evaluated.

MATERIAL AND METHODS

In this section, general information is given about technical structures in which used in the system at FPGA chip, chaotic systems, fixed and floating point number systems.

Fixed and Floating Number Systems and Modified Chua Chaotic Oscillator

The whole universe is moved with frequency domain. In this direction frequency and signal processing methods form the basis of each electronically systems. Digital signal processing methods move with two essential number bases as fixed point bases and floating point bases. These number systems thought storing methods and transmission methods of computer-based data. The floating point number system represents the large scale according to a fixed point. This situation not only represents to maximum and minimum range of number value but also the width of the range of decimal values is also represented. While floating point number system using more resources on the chips, the fixed point number system was seen more economical.

The mathematical function of the Modified Chua chaotic system is represented by the system of differential equations (1), where p_1, p_2, p_3, p_4 are the four state variables and σ, γ, θ, c, d are the system coefficients.

$$\begin{aligned}
\frac{dp_1}{dt} &= -g(p_1, p_3)(p_1 - p_3) - p_2, \\
\frac{dp_2}{dt} &= p_1 + \gamma p_2, \\
\frac{dp_3}{dt} &= \theta\left(g(p_1, p_3)(p_1 - p_3) - p_4\right), \\
\frac{dp_4}{dt} &= \sigma p_3.
\end{aligned} \tag{1}$$

$g(p_1, p_3)$ is a nonlinear function with the parameters c and d, as defined in Equation (2).

$$g(p_1, p_3) = c(p_1 - p_3 - d)(p_1 - p_3) > d(p_1 - p_3) \leq d \tag{2}$$

The Forward Euler method is one of the most important numerical analysis techniques. It is commonly used for the numerical analysis of differential equations, which are employed to model changing variables in dynamic systems, such as chaotic systems. The essential principle of the Forward Euler method involves updating system variables regularly. This step-by-step process predicts changes in the system variables between discrete time steps.

Table 1 Floating and fixed point-based chaotic oscillators on FPGA in literature

Study	Chaotic Generator	Max. Operating Frequency (MHz)	Numerical Method	Platform	Number System
Fei Yu (2020)	Modified Chua	180.180	RK4	Xilinx ZYNQ-XC7Z020	32-bit Floating Point
Murat Tuna (2019)	Lu-Chen	464.688	Heun	Xilinx Virtex-6	32-bit Floating Point
Mohamed Salah Azzaz (2013)	Lorenz	38.86	Euler	Xilinx Virtex-2	32-bit Floating Point
Mohammed F. Tolba (2017)	Liu	137.561	Fractional order	Xilinx Virtex-5	Fixed Point
Sadoudi Said (2009)	Chen	22.850	RK4	Xilinx Virtex-2	32-bit Floating Point
Luciana De Micco (2011)	Lorenz	3.676 - 125	RK4	Altera Cyclone-III	32-bit Floating Point
Akif Akgul (2015)	Lorenz	373.134	RK4	Xilinx ISE and Labview Simulator	32-bit Floating Point
E. Tlelo-Cuautle (2015)	Chua	70.943, 69.500, 58.648, 48.209	RK4 / Forward Euler	Xilinx Spartan-3	Fixed Point
Omar Guillén-Fernández (2021)	CO1, CO2, CO3, HO4, HO5	90.88, 102.75, 58.55, 79.77, 82.7	Forward Euler	Altera Cyclone-IV	Fixed Point
Present	Modified Chua	273.631 - 50.242	Forward Euler	Xilinx Virtex-6	Floating Point and Fixed Point

The Forward Euler method can be expressed with a simple equation:

$$y_{n+1} = y_n + h \cdot f(t_n, y_n) \tag{3}$$

Different initial conditions and system parameter values can be used for the Modified Chua system to exhibit the desired nonlinear dynamic behavior. The initial conditions and parameters used in this study for the implementation of the Modified Chua chaotic system are provided in Table 2.

Table 2 Initial Conditions and System Parameters of the Modified Chua Chaotic System

Initial Conditions				Parameters				
p_1	p_2	p_3	p_4	σ	γ	θ	c	d
0.1415	-2.073	-0.252	0.829	0.5	10	1.5	3	1

The Modified Chua chaotic system has been modeled numerically using the Euler algorithm. Figure 1 shows the phase portraits of the system state variables. Figure 2 shows the time series of the system state variables. For the mathematical calculations of the Modified Chua chaotic oscillator, the step size of the algorithm is chosen as $h = 0.005$. For $k = 0$, the initial values are set to $P_1(k) = 0.1415$, $P_2(k) = -2.073$, $P_3(k) = -0.252$, and $P_4(k) = 0.829$. The system parameters are considered as $\sigma = 0.5$, $\gamma = 10$, and $\theta = 1.5$.

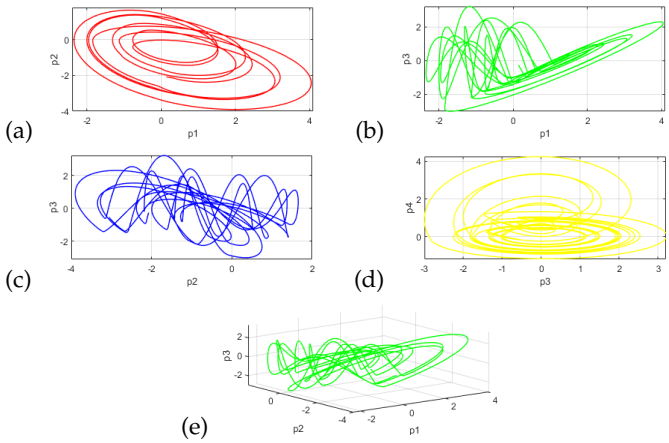

Figure 1 The phase portraits of the Modified Chua chaotic system state variables: (a) p_1-p_2, (b) p_1-p_3, (c) p_2-p_3, (d) p_3-p_4, (e) p_1-p_2-p_3.

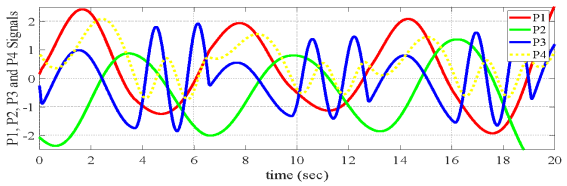

Figure 2 The time series of the Modified Chua chaotic system state variables for P_1, P_2, P_3, and P_4.

FPGA-Based Modified Chua Chaotic System

FPGA chips are widely used for low power consumption, reprogrammability, fast prototyping, and parallel signal processing capabilities in academic and industrial fields. FPGA chips are designed with languages such as VHDL, Verilog, and System C. Compared to specially designed graphics cards, supercomputers, and parallel computers, these chips are low-cost and easier to access. Chaotic systems are one of the very sensitive areas in digital signal processing. This sensitivity and the high energy consumption caused by it can be mitigated with the parallel processing and low power consumption capabilities of FPGA chips.

Figure 3 shows the parts of a basic FPGA chip. A basic FPGA chip consists of three main components: Configurable Logic Block (CLB), Input-Output Blocks (IOBs), and interconnections. According to the digital circuit designed by the user, the logic blocks and the connections between them are configured. The CLB provides functional elements for the logic circuit that the user wants to create. The IOB provides an interface between the internal signal lines of the chip and the pins of the chip. Interconnections are used for configuring the connections between the CLB and IOB.

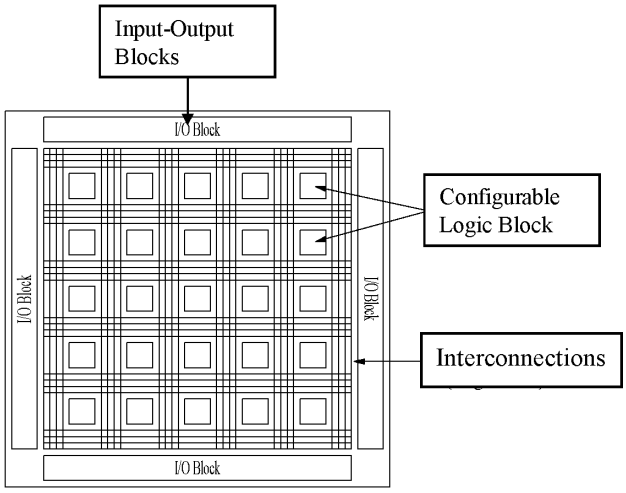

Figure 3 The parts of a basic FPGA chip: Configurable Logic Block (CLB), Input-Output Blocks (IOBs), and interconnections.

Chaotic systems exhibit complex behavior without any particular order or predictability. They are dynamical systems that can be expressed in terms of nonlinear equations and can respond to small changes over time. One of the most important things is that tiny changes at initial conditions can have enormous effects over time. Because of these effects, chaotic systems need not only memory space but also parallelism to calculate fast on generating new values. Therefore FPGA chips are generally preferred for chaotic systems. The Chua circuit is an electrical circuit using passive elements such as resistors, capacitors, and active elements such as diodes, transistors, and amplifiers. This circuit is a system that can exhibit chaotic behavior under certain conditions.

FPGA-BASED CHAOTIC SYSTEMS

In this section, the structure of the Modified Chua chaotic oscillator is described using both floating-point and fixed-point bases. The 32-bit IEEE-754-1985 single-precision standard is used for floating-point number representation, while the 16I-16Q format is used for IQ-Math with fixed-point numbers.

Fixed Point Based Modified Chua Chaotic Oscillator Unit on FPGA

Fixed-point implementation for fractional calculus in FPGA is the most straightforward approach since it uses a predefined number of bits for all of the signal nets. From the perspective of FPGA, the system works with binary numbers without knowing about fraction points; it is implemented in the initial design stage and therefore does not require any additional resources for calculation processing, unlike floating-point format. In the present work, 32 bits are used, from which 1 bit is reserved for the sign, 15 bits for representing integer values, and 16 bits for representing fractional values. This way, such a format can represent numbers from $-2^{15} = -32768$ to $(2^{15} - 2^{-16}) = 32767.99998474121$ with precision equal to $2^{-16} = 1.52587890625 \times 10^{-5}$. The integer part has a large reserve for further processing needs, while the fractional part, which limits the absolute maximum number of chaos discrete values, provides acceptably high precision values for the obtained chaos to exhibit itself.

To implement the continuous chaotic system in a digital system, the ordinary differential equations need to be solved using some discrete integration method. In this work, the forward Euler method is used for fixed-point Modified Chua chaos generator implementation, with a time step of $1/1024$. Other methods (such as 4th order Runge-Kutta) may provide more accurate results in some cases but are more complex to implement and require more hardware resources. Since with the chosen integration time step and method, the solutions of the chaos system's differential equations always converge, this approach is feasible for practical use in experimental studies. The Matlab Simulink model of the fixed-point based Modified Chua oscillator is shown in Figure 4.

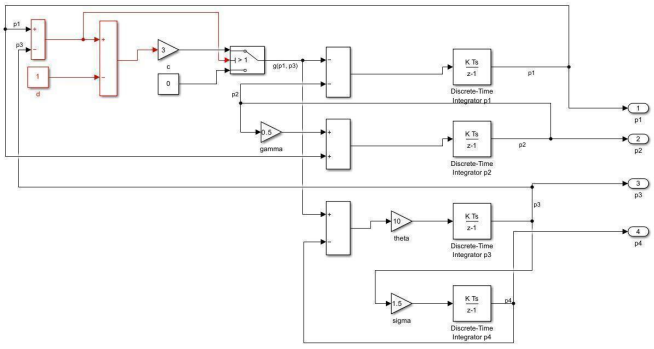

Figure 4 Matlab Simulink model of the fixed-point based Modified Chua chaotic oscillator.

The Modified Chua chaotic oscillator has been designed in Matlab Simulink, and the design has been verified to work as expected. After this step, the VHDL code was generated using the Matlab HDL Coder Toolbox. In this study, the fixed-point number standard was used for converting the model in Matlab Simulink into VHDL language. A testbench was designed and tested using Xilinx ISE Design Tools to verify the design. The test results of the fixed-point based Modified Chua chaotic oscillator are shown in Figure 5.

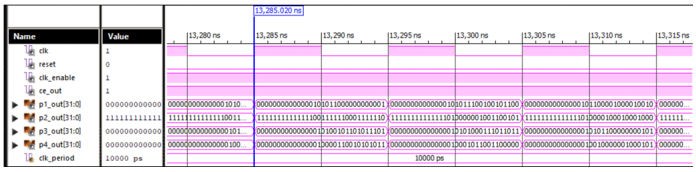

Figure 5 Modified Chua chaotic oscillator test results based on fixed point obtained from Xilinx ISE Design Tools.

Figure 6 shows the top-level block diagram of the fixed-point implementation of the Modified Chua chaotic oscillator unit. This unit has three inputs: a 1-bit *clk*, a 1-bit *clk_enable*, and a 1-bit *reset*. It also has five outputs: 32-bit *P1_out*, *P2_out*, *P3_out*, *P4_out*, and a 1-bit *ce_out*. When the *clk* signal has a rising edge, the system is activated and generates new values. The chaotic signal values are output through *P1_out*, *P2_out*, *P3_out*, and *P4_out*, and the system's functionality is verified by monitoring the output of the *ce_out* signal. The schematic for the second-level blocks is not presented due to its complexity and overly detailed nature.

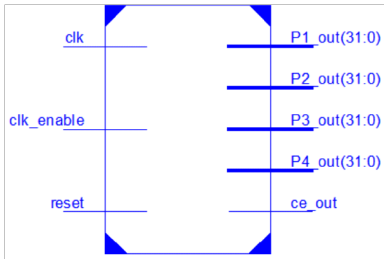

Figure 6 Top-level block diagram of the fixed-point based Modified Chua chaotic oscillator unit on FPGA.

The VIRTEX-6 ML605 FPGA evaluation board (Device: XC6VLX240T, Package: FF1156, Speed: -1) was used for the implementation. The maximum operating frequency for the design was 50.242 MHz. FPGA utilization statistics and the maximum frequency for the fixed-point implementation of the Modified Chua chaotic oscillator unit are presented in Table 3.

A testbench was written in VHDL language to analyze the results generated by the fixed-point based Modified Chua chaotic oscillator for the P_1, P_2, P_3, and P_4 signals. The design was run in the Xilinx ISE Design Suite, and 4,000 values for each signal were saved in a .txt file. The related values were converted to real values to generate the time series graph. The time series of the Modified Chua chaotic oscillator for P_1, P_2, P_3, and P_4 signals are shown in Figure 7.

Floating Point Based Modified Chua Chaotic Oscillator Unit on FPGA

In this section, the discretized model of the Modified Chua chaotic system is obtained using the Euler numerical differential equation

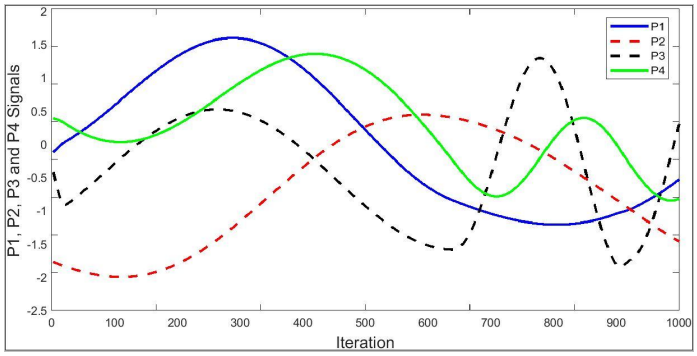

Figure 7 Time series of the fixed-point based Modified Chua chaotic system for P_1, P_2, P_3, and P_4 signals on FPGA.

solution method. Next, the related chaotic system is designed using VHDL and Xilinx ISE Design Tools. After the design process, the chaotic system is tested with a testbench written in VHDL and using Xilinx ISE Design Tools to verify the Floating Point based Modified Chua Chaotic Oscillator unit. The chip statistics for the Floating Point based Modified Chua Chaotic Oscillator unit are presented. The top-level block diagram of the floating-point based Modified Chua Chaotic Oscillator Unit on FPGA is shown in Figure 8.

The top-level block diagram includes a 1-bit *clk*, *Reset*, and *Start* signals as inputs, and 32-bit *P1_out*, *P2_out*, *P3_out*, *P4_out*, and a 1-bit *Result_Ready* signal as outputs.

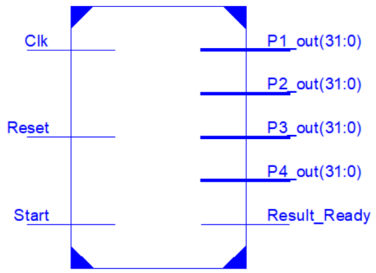

Figure 8 Top-level block diagram of the floating-point based Modified Chua Chaotic Oscillator Unit on FPGA.

Figure 9 shows the second-level block diagram of the floating-point based *Modified_Chua_Euler* unit. This includes *x4mux* and *Modified_Chua_Euler* units in the second-level design. The *x4mux* unit has inputs grouped as 32-bit 2X4. The first four groups represent the initial conditions required for starting operation. When the *Modified_Chua_Euler* unit begins generating results, the second four groups send all data either to the system output as *P1_out*, *P2_out*, *P3_out*, *P4_out* or to the *x4mux* unit as the next initial conditions. The *shys* signal is used as a control process. When the value of *shys* is '0', the *x4mux* unit sends initial conditions to the *Modified_Chua_Euler* unit. If the value of *shys* is '1', the *x4mux* unit sends the generated values to the *Modified_Chua_Euler* unit.

The third-level block schematic for the floating-point based *Modified Chua Chaotic Oscillator* unit is shown in Figure 10. The design includes IP-Core units, a *modified_Chua_core* unit, and a filter unit for multiplication and addition operations in 32-bit floating-point standards. The *Modified_Chua_core* unit and the Chua chaotic system are implemented in VHDL for FPGA realization. The filter unit is created to prevent unintended consequences of the *Chua_Chaotic_Oscillator* unit.

Table 3 FPGA utilization statistics of the fixed-point based Modified Chua Chaotic Oscillator Unit

	Number of Slice Registers	Number of Slice LUTs	Number of Occupied Slices	Number of DSP48E1s	Number of IOBs	Maximum Clock Frequency (MHz)
Used	128	642	158	8	132	
Utilization (%)	1	1	1	1	22	50.242
Available	301,440	150,720	37,680	768	600	

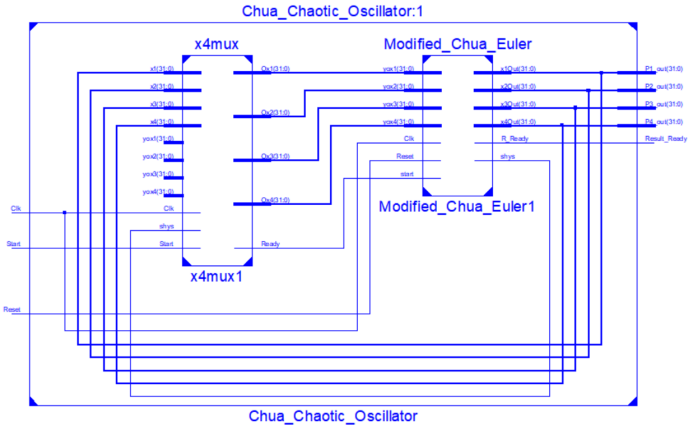

Figure 9 Second-level block diagram of the floating-point based Modified Chua Chaotic Oscillator Unit on FPGA.

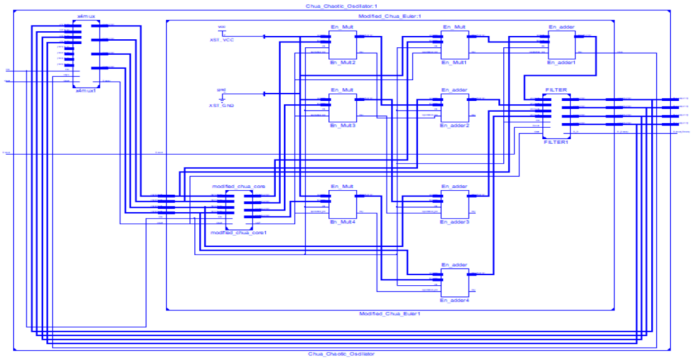

Figure 10 Third-level block diagram of the floating-point based Modified Chua Chaotic Oscillator Unit on FPGA.

The simulation results of the floating-point based *Modified Chua Chaotic Oscillator* unit are shown in Figure 11. The designed unit sends signals to the outputs (*P1_out*, *P2_out*, *P3_out*, and *P4_out*) on every 69th clock pulse. While the *Chua_Chaotic_Oscillator* unit is generating results, the *Result_Ready* signal is set to '1'; otherwise, it remains '0'.

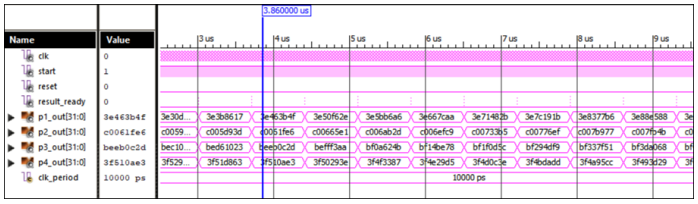

Figure 11 Simulation results of the floating-point based Modified Chua Chaotic Oscillator unit on FPGA.

FPGA utilization statistics and the maximum frequency have been presented for the realization of the floating-point based *Modified Chua Chaotic Oscillator* unit in FPGA. The VIRTEX-6 ML605 (Device: XC6VLX240T, Package: FF1156, Speed: -1) evaluation board was used for realization, achieving a maximum frequency of 273.631 MHz. The results are shown in Table 4.

A testbench was written in VHDL language to analyze the results generated by the floating-point based Modified Chua chaotic oscillator for the P_1, P_2, P_3, and P_4 signals. The design was run in the Xilinx ISE Design Suite, and 4,000 values for each signal were saved in a .txt file. The related values were converted to real values to generate the time series graph. The time series of the Modified Chua chaotic oscillator for P_1, P_2, P_3, and P_4 signals are shown in Figure 12.

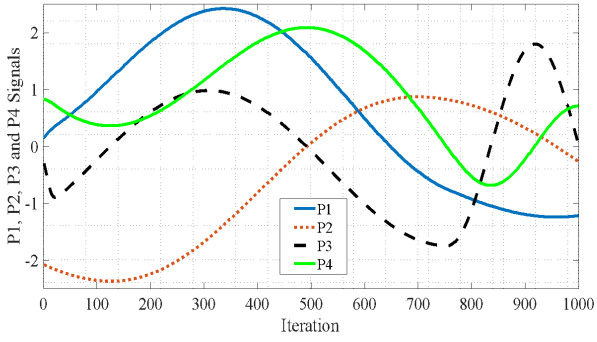

Figure 12 Time series of the floating-point based Modified Chua chaotic oscillator for P_1, P_2, P_3, and P_4 signals on FPGA.

Table 4 FPGA utilization statistics of the floating-point based Modified Chua Chaotic Oscillator Unit

	Number of Slice Registers	Number of Slice LUTs	Number of Occupied Slices	Number of DSP48E1s	Number of IOBs	Maximum Clock Frequency (MHz)
Used	6,827	6,395	2,325	9	132	
Utilization (%)	2	4	6	1	22	273.631
Available	301,440	150,720	37,680	768	600	

CONCLUSION

In this study, the Modified Chua chaotic system has been designed using the 32-bit IQ-Math number system and the 32-bit IEEE-754-1985 standard for implementation on FPGA chips. The Modified Chua chaotic oscillator based on the floating-point number system was designed using VHDL, while the fixed-point version was modeled in Matlab Simulink and then converted to VHDL using the Matlab HDL Coder Toolbox. Both designs of the Modified Chua chaotic oscillators were tested using a testbench composed in VHDL, and the successful simulation results were presented in this study.

The two designs of the Modified Chua chaotic oscillators were synthesized with the Xilinx ISE Design Tools 14.2 for the Virtex-6 chip on the ML605 FPGA development board. The fixed-point based Modified Chua chaotic system achieved a maximum frequency of 50.242 MHz, while the floating-point based version achieved a maximum frequency of 273.631 MHz. Although the floating-point design provided a higher maximum frequency, the fixed-point design was more favorable in terms of resource utilization.

With the findings presented in this study, a high-speed random number generator can be developed using the floating-point based Chua chaotic oscillator. Furthermore, a low-cost, customized FPGA-based chaotic random number generator can be implemented using the fixed-point based Chua chaotic oscillator. It has been demonstrated that the Modified Chua chaotic oscillators based on both floating and fixed-point number systems can be used safely in secure communication and cryptographic applications. In future studies, a random number generator may be developed for secure communication and cryptographic applications using FPGA-based Modified Chua chaotic oscillators designed with both number systems.

Availability of data and material

Not applicable.

Conflicts of interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

Ethical standard

The authors have no relevant financial or non-financial interests to disclose.

LITERATURE CITED

Akif Akgul, H. C., 2015 Chaos-based engineering applications with a 3d chaotic system without equilibrium points. Nonlinear Dynamics .

Amir Anees, I. H., 2018 A novel method to identify initial values of chaotic maps in cyber security. MDPI .

Arpaci, B., 2019 *Color Image Encryption System Designed with The Modified Chua Circuit For Security Data Transmission*. Ph.D. thesis, Gazi University, Ankara.

E. Tlelo-Cuautle, J. R.-M.-A.-R.-P., 2015 Fpga realization of multi-scroll chaotic oscillators. Communications in Nonlinear Science and Numerical Simulation **27**: 66–80.

Erkan Tanyıldızı, T. C., 2017 Kaotik haritalı balina optimizasyon algoritmaları. Science and Engineering Journal of Fırat University pp. 307–317.

Fatih Karataş, K., 2020 Implementation of fuzzy logic membership functions on fpga. Bilgisayar Bilimleri ve Teknolojileri Dergisi pp. 1–9.

Fatih Karataş, K., 2021 Design and implementation of fpga-based arrhythmic ecg signals using vhdl for biomedical calibration applications. International Advanced Researches and Engineering Journal pp. 362–371.

Fatih Özkaynak, A. B., 2013 Security analysis of an image encryption algorithm based on chaos and dna encoding. IEEE .

Fei Yu, H. S., 2020 Ccii and fpga realization: A multistable modified fourth-order autonomous chua's chaotic system with coexisting multiple attractors. Complexity, Dynamics, Control, and Applications of Nonlinear Systems with Multistability pp. 1–17.

Filips Capligins, A. L., 2021 Fpga implementation and study of synchronization of modified chua's circuit-based chaotic oscillator for high-speed secure communications. In *IEEE 8th Workshop on Advances in Information, Electronic And Electrical Engineering*.

Gabr, M. K., 2023 *Image Encryption Based On Base-N PRNGs Key Application And Parallel Base-N S-Boxes*. The German University, Cairo.

Jorge Pomares, I. P., 2014 Dynamic visual servoing with chaos control for redundant robots. IEEE/ASME Transactions On Mechatronics pp. 423–430.

Koyuncu, T. M. F.-A.-M.-T.-M. C. E., I., 2022 Real time realization of image processing algorithms on fpga. Journal of BAUN Institute of Science and Technology **24**: 125–137.

Linsheng Zhang, Y. Z., 2009 Floating-point to fixed-point transformation using extreme value theory. In *IEEE/ACIS International Conference on Computer and Information Science*, pp. 271–276.

Litvinenko, A., 2017a *Use of Chaotic Sequences For Data Transmission System*. Riga Technical University.

Litvinenko, A., 2017b *Use of Chaotic Sequences for Data Transmission Systems*. Ph.D. thesis, Riga Technical University, Faculty of Elec-

tronics and Telecommunications, Institute of Radioelectronics.
Litvinenko, A. and A. A., 2019 Advanced chaos shift keying based on a modified chua's circuit. In *IEEE Microwave Theory And Techniques In Wireless Communications (MTTW)*, pp. 17–22.
Luciana De Micco, H. A., 2011 Fpga implementation of a chaotic oscillator using rk4 method. In *Southern Conference On Programmable Logic*, pp. 185–190.
Mohamed L. Barakat, A. S., 2013 Hardware stream cipher with controllable chaos generator for colour image encryption. IETL .
Mohamed Salah Azzaz, C. T., 2013 A new auto-switched chaotic system and its fpga implementation. Communications in Nonlinear Science and Numerical Simulation pp. 1792–1804.
Mohammed F. Tolba, A. M., 2017 Fpga implementation of two fractional orders chaotic systems. AEU-International Journal of Electronics and Communications **78**: 162–172.
Murat Alcin, I. P., 2016 Hardware design and implementation of a novel ann-based chaotic generator in fpga. Elsevier pp. 37–58.
Murat Tuna, M. A., 2019 High speed fpga-based chaotic oscillator design. Microprocessors and Microsystems **73–80**.
Omar Guillén-Fernández, M. F.-L.-C., 2021 Issues on applying one- and multi-step numerical methods to chaotic oscillators for fpga implementation. Mathematics .
Ruslans Babajans, D. D., 2020 Noise immunity of substitution method-based chaos synchronization in vilnius oscillator. IEEE Microwave Th and Techniq in Wireless Communications .
Sadoudi Said, M. S., 2009 An fpga real-time implementation of the chen's chaotic system for securing chaotic communications. International Journal of Nonlinear Science pp. 467–474.
Taşdemir, I. K., M. F., 2020 Real-time fast corner detection algorithm based image processing application on fpga. In *International Asian Congress on Contemporary Sciences-III*, pp. 39–46, Konya.
Vasyuta, K., F. Zots, and I. Zakharchenko, 2019 Building the air defense covert information and measuring system based on orthogonal chaotic signals. Peer-Reviewed Open Access Scientific Journal pp. 33–43.
Zhengxing Huang, W. D., 2014 Similarity measure between patient traces for clinical pathway analysis: Problem, method, and applications. IEEE Journal of Biomedical and Health Informatics pp. 4–14.

How to cite this article: Taşdemir, M. F., Litvinenko, A., Koyuncu, I., and Capligins, F. Performance Evaluation of FPGA-Based Design of Modified Chua Oscillator. *Chaos Theory and Applications*, 6(4), 249-256, 2024.