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RESEARCH ARTICLE

MODELING AND PERFORMANCE ANALYSIS OF HIGH BANDWIDTH TRANSIMPEDANCE AMPLIFIERS IN OPTICAL COMMUNICATIONS

Berkay ÇAVUŞ [1,*], Şekip Esat HAYBER [2]

[1] Department of Electrical-Electronic Engineering, Engineering Faculty, Bursa Uludağ University, Bursa, Turkey
berkaycavus@gmail.com - 0009-0007-1184-8807

[2] Department of Electrical-Electronic Engineering, Engineering Faculty, Bursa Uludağ University, Bursa, Turkey
sehayber@uludag.edu.tr - 0000-0003-0062-3817

Abstract

This study aims to optimize the performance of optical communication and sensing systems using avalanche photodiodes (APD) and transimpedance amplifiers (TIA). The high gain of APDs at low light levels and TIA circuits' wide bandwidth, low noise, and high-speed characteristics are critical for these applications. In the design process, a T feedback network and various operational amplifiers were used to enhance the performance of the TIA circuit. LTspice simulations examined the effects of white noise on the circuit's current and output voltage and the noise performance under various noise divider values. The impact of changes due to laser distance and dark current were also analyzed. These analyses reveal how the TIA circuit achieves high performance in different applications and demonstrates the effectiveness of noise reduction techniques. The results provide significant insights into the design of TIA circuits used in optical communication and sensing systems.

Keywords

Transimpedance amplifier (TIA),
Avalanche photodiodes (APD),
Optical communication,
Sensing systems,
T feedback network

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1. INTRODUCTION

Rapid advances in optical communication technologies in recent years have highlighted the importance of optical receivers, crucial components for converting optical signals into electrical signals in communication and sensing systems [1]. A core component of these receivers, the transimpedance amplifier (TIA), is employed in diverse applications, including optical communication (e.g., 2.5, 10, and 25 Gb/s), mechanical sensors, biosensors, DNA sequencing, impedance spectroscopy, and remote sensing [2,3]. This extensive application range introduces various technical challenges for TIA circuit designers, such as achieving GHz-level bandwidth in communication systems while optimizing noise performance in lower-frequency bioapplications [4,5,6]. Furthermore, low power consumption is essential for bio-implantable applications, highlighting the need for high flexibility and performance optimization in TIA design [5,7].

In critical applications, noise signals can interfere with accurate signal detection, especially in low-light environments. For instance, shallow current signals are produced at photodetector outputs in remote sensing applications such as LIDAR (light detection and ranging) [8,9]. TIA circuits, particularly when paired with avalanche photodiodes (APDs), help address these challenges, enabling efficient signal processing in such conditions [10].

*Corresponding Author: berkaycavus@gmail.com

TIA circuits also possess other essential features, including wide bandwidth, fast response time, and adjustable gain for application-specific sensitivity. These features are especially valuable in optical communication, where modern TIAs deliver high performance, critical for energy efficiency [5,11]. Additionally, TIAs support APDs to operate effectively, thereby enhancing the performance of optical communication systems and other optoelectronic applications.

Recently, the significance of APD and TIA circuits has increased in optical communication and sensor technologies, including applications like short-range LIDAR sensors with on-chip APDs fabricated using CMOS technology [12]. Such receivers show significant potential, particularly in indoor monitoring applications [13]. In data computing, dense wavelength multiplexing (DWDM) connections have been studied to overcome electronic connection limitations and meet data traffic demands [14]. Moreover, multi-channel analog front-end circuits have been developed for linear LADAR applications, underscoring the critical role of APD and TIA circuits in advancing optical communication and sensor technologies [12,15].

This study aims to design an optimized TIA circuit for APDs that provides high sensitivity, low noise, high speed capabilities and cost-effective performance to meet the increasing demands in optical communication and sensor technologies, and also contributes to the performance of transimpedance amplifiers (TIAs) by addressing several important issues that are often neglected in the existing literature. Simulation analyses evaluate the ability of the circuit to accurately process signals at different frequencies by considering variables such as laser distance and dark current effects. First, the effects of white noise intensities and feedback capacitor values on the performance of the TIA circuit are modeled and a comprehensive analysis is presented. In addition, performance enhancement is achieved under various operating conditions thanks to the noise reduction techniques integrated into the TIA design. In addition, an innovative approach is demonstrated in the TIA circuit design by using a T feedback network and different operational amplifiers. This study, in which variables such as laser distance and dark current effects are evaluated by simulation analyses, examines the ability of the TIA circuit to accurately process signals at various frequencies in detail. These unique contributions make the study stand out from the existing literature and an important step towards meeting the increasing demands in optical communication and sensor technologies at a low cost.

2. MATERIAL AND METHOD

APDs are semiconductor devices that provide high sensitivity and fast response times. Multiplying the electron-hole pairs formed by light photons with the Lavin effect provides substantial signal gains even at low light levels [11]. Excelitas' C30737 series APDs offer high sensitivity, especially at wavelengths between 500 nm and 1000 nm, making them an ideal choice for automotive LIDAR, laser meter, and area scanning applications [16]. When designing a suitable TIA circuit for APDs, attention should be paid to the electrical and optical properties of the APD. This circuit converts the current signal from the APD into a voltage signal [12]. For Excelitas C30737 series APDs, the low bias voltage is necessary for the APD to provide high gain. Additionally, the fast response time (about 200 ps) and low noise level (about 0.1 pA/√Hz) of APD should be considered in TIA circuit design [16]. The wide bandwidth and high sampling rate of the TIA circuit must be compatible with the high cutoff frequency (>1 GHz) of the APD [15].

At wavelengths of 800 nm and 900 nm, the reverse bias voltage directly affects the gain of the APD. For 800 nm, the typical breakdown voltage varies between 120V and 210V, while for 900 nm, this range is between 180V and 260V [16]. The reverse bias voltage should be set at the optimal point higher than these breakdown voltages but before the Lavin effect begins. This provides efficient signal amplification and prevents overheating and device damage [11]. The gain values of the APD also vary depending on the wavelength, so these factors should be considered when choosing the reverse bias voltage [16]. Other essential features to consider in the design of an APD-based TIA circuit include the bandwidth of the

circuit, the sampling rate, and the capacitance of the APD [12]. The capacitance values of Excelitas C30737 series APDs vary depending on the bias voltage, which can affect the bandwidth and noise performance of the TIA circuit [16]. The pulse width of the APD determines the shortest signal duration that can be detected by the system, which is especially critical in applications requiring fast response [15]. The ideal OpAmp selection for TIA circuits depends on the application's requirements. The following OpAmp models are generally preferred for scenarios requiring low noise, speed, and high sensitivity, such as APD applications:

Texas Instruments OPA657, 1.6 GHz gain-bandwidth multiplication, low noise (4.8 nV/√Hz), and 700 V/µs slew rate. In addition to being perfect for high-speed applications and has wide bandwidth [17]. Analog Devices AD8009, 5.175 GHz gain bandwidth multiplication, and 5500 V/µs slew rate. The high slew rate is ideal for high-speed signal processing [18]. Texas Instruments THS3001, 420 MHz, provides bandwidth, low noise, and a 6500 V/µs slew rate. High power output driver and very high rotation speed, compatible with a wide range of loads [19]. Analog Devices LTC6268, with 500 MHz gain bandwidth multiplication and low input bias current in the femtoampere range. High-speed combination with ultra-low input bias current, good compatibility with capacitive loads [20].

At this point, LTC6268 was chosen. The LTC6268 is the operational amplifier in transimpedance circuits designed for APDs. The reasons for this choice stem from the fact that the set of features that the LTC6268 combines are ideal for applications that require high sensitivity and fast response [23]. In addition to these functional advantages, the selection of LTC6268 was also guided by its cost-effectiveness and ease of integration into compact circuit designs. First, the ultra-low input bias current at the femtoampere level enables precise measurements by reducing voltage errors in signals received from high-impedance sensors [20]. Moreover, with its high slew rate of 1.25 V/µs, the LTC6268 can effectively process rapidly changing signals, maintaining integrity under dynamic signal conditions. This model, which comes with a low noise level (4.3 nV/√Hz), makes obtaining clear and sharp signal outputs possible by minimizing noise, especially at low signal levels. Finally, the wide gain bandwidth of 500 MHz delivers the performance required for high-frequency applications, and the LTC6268's compatibility with capacitive loads simplifies the circuit design. These features make the LTC6268 a reliable choice in critical applications such as optoelectronic sensing systems.

The TIA circuit is a circuit with an OpAmp and a feedback resistor. The current input is received from a photodetector or similar sensor. This incoming current is directed to the reverse input of the circuit, where it is converted into a low-impedance voltage signal by the OpAmp using negative feedback. The feedback resistor determines the relationship between output voltage and input current. The larger this resistor, the greater the output voltage the TIA produces. Using the "T feedback network" design for TIA improves the circuit's performance by providing several advantages. The T feedback network is a structure usually consisting of a resistor and two capacitors and when integrated into the OpAmp circuit, provides the following benefits:

- T feedback network is used to extend the bandwidth of the OpAmp. This structure limits the OpAmp's low-frequency gain while providing a flatter gain profile at high frequencies. This helps maintain the signal's integrity, especially in optoelectronic applications that require high-speed processing.
- The T-network allows the OpAmp to handle positive and negative charge capacitances. Thus, it supports the circuit's more stable operation and compatibility with capacitive loads. This stability reduces signal fluctuations and is especially important in applications where dynamic signal changes occur frequently.
- Effectively reduces noise levels and prevents potential emissions. While capacitors help filter unwanted peaks that may occur at high frequencies, the resistor prevents overreactions by slowing down the overall response of the circuit.

- It helps to harmonize the circuit's input and output impedances with other electronic components to which it is connected. This reduces signal loss and provides higher efficiency during data transmission.
- Using the T feedback network allows the OpAmp circuit to operate more comprehensively. This is especially important for sensors operating in various light conditions because the circuit can more accurately process multiple signals.

It should be noted that in designing the T feedback network, the selection of capacitor and resistor values is crucial, as they directly impact bandwidth and noise performance. These values were carefully optimized through iterative simulations to achieve the desired gain and noise reduction levels suitable for high-speed and precision sensing applications. It is integrated with a high-performance OpAmp, such as the LTC6268, which maximizes overall system performance by offering low noise and high stability while increasing the circuit's ability to collect fast data. How accurately TIAs work depends on signal conditioning, linearity, hysteresis, and temperature. Depending on the intended use and environmental conditions, adding extra circuit elements, such as noise-reducing filters, may be necessary for higher accuracy. Active filter techniques or passive filters containing resistors and capacitors can be used on the circuit output to eliminate unwanted signals. A unique amplifier, the TIA, corrects minimal currents in the reverse direction. The designed circuit is shown in Figure 1.

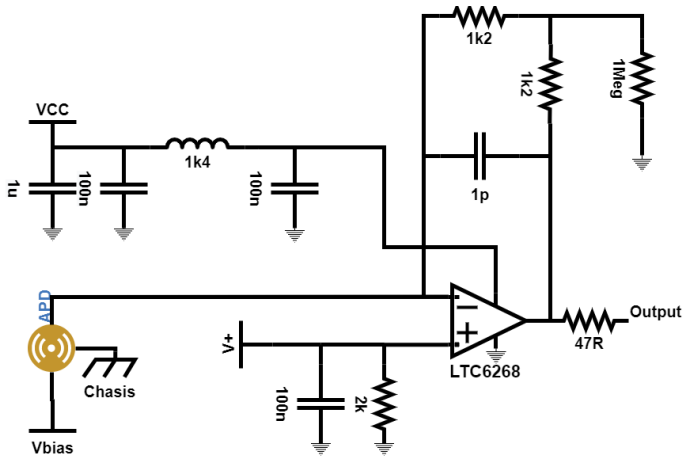

Figure 1. TIA circuit design.

A Ferrite bead is a circuit element whose impedance increases at high frequency. The value "1k4" indicates that the ferrite bead has an impedance of 1.4 kΩ at high frequency. Ferrite bead absorbs high-frequency noise and converts energy into heat, effectively blocking frequencies in the range of 100 kHz to several hundred MHz. In this design, frequencies around 98 kHz and 326 kHz are specifically targeted, as they often correspond to noise generated by switching power supplies (SMPS) and other industrial sources. By filtering out these frequencies, the ferrite bead reduces the impact of switching harmonics and external electromagnetic interference (EMI) on the circuit. This prevents high-frequency noise on the feed line from reaching the operational amplifier. Capacitors are usually added parallel to an operational amplifier's supply leg to further enhance noise suppression. For instance, the combination of 100 nF and 1 uF capacitors in this circuit helps to target different noise bands, with the 100 nF capacitor focusing on higher frequencies (such as 100 kHz and above) and the 1 uF capacitor addressing lower-frequency noise components. This is to filter out high-frequency noise in the feed line. Capacitors direct this noise to the ground by creating a low impedance path at high frequency. Capacitors of different values are used to filter noise in different frequency ranges, effectively isolating sensitive components from noise within the 98 kHz to 326 kHz band, which is commonly associated with external RF interference and switching noise. The block diagram of the designed system is shown in Figure 2.

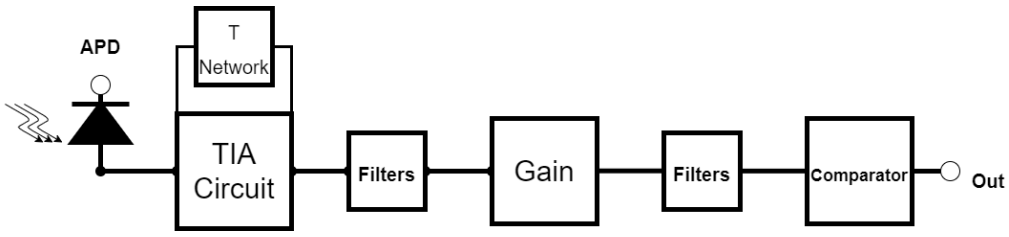

Figure 2. Block diagram of the system.

Additionally, the APD was supplied with reverse voltage. The use of this reverse bias voltage plays a critical role in maximizing the performance of the APD. Reverse bias reduces the internal capacitance of these detectors, speeding up their response time and increasing their internal gain through the pulse multiplying effect. These features are essential, especially in high-speed and precise optical detection applications. Thus, the combination of reverse bias application and T feedback network enables more accurate and faster processing of signals received from APD or photodiodes, significantly improving the overall system performance.

However, when we try to sample the output voltage obtained only with TIA with the help of MCU, we cannot get sufficient resolution. Therefore, we must add a gain stage to this circuit design to increase the voltage of this output. Operational amplifiers are essential signal-processing components in electronic circuits and typically perform signal amplification functions. The gain factor of an OpAmp is determined by the passive components included in the circuit and acting as a feedback network. In this phase of the study, a non-inverting configuration was used. On the other hand, a non-inverting gain circuit is a configuration in which the input signal is applied to the positive terminal of the amplifier, and the output is realized as a copy of the input signal with the same phase and amplitude. The following equation determines the voltage gain, A_v of this circuit configuration:

$$A_v = 1 + \left(R_f / R_{in}\right) \tag{1}$$

Here, A_v is the voltage gain, R_f is the feedback resistor, and R_{in} is the input resistance. This signal can be routed to an operational amplifier gain circuit to increase the gain of the signal obtained from a TIA output. Feedback and input resistors must be carefully selected in this integration process to achieve predetermined gain values. In this case, our gain is A_v=11.

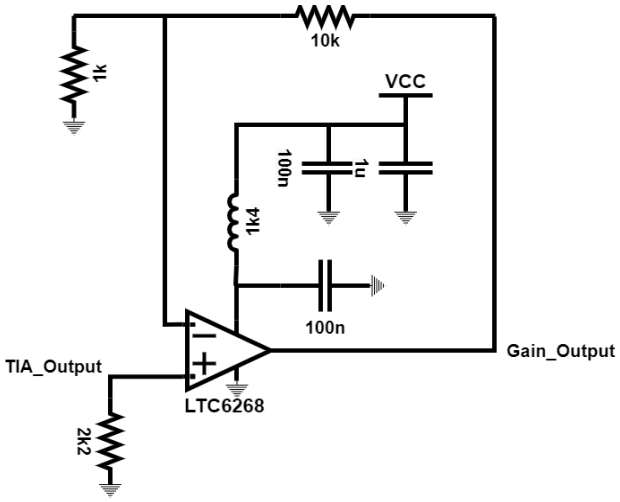

Figure 3. Gain circuit design.

This flyback converter circuit is selected to provide the -60V reverse bias voltage required for driving the APD and is ideal for applications requiring isolated power conversion. In this design, the FQP30N06L MOSFET is driven by a PWM signal to achieve high-speed switching on the primary winding of the transformer. The FQP30N06L was chosen for its low on-resistance and high switching speed, which enhance the converter's efficiency and make it suitable for high-frequency operation. The PWM control circuit ensures accurate timing of the MOSFET switching, providing a stable and continuous output voltage. The transformer not only enables voltage conversion but also adds isolation to improve circuit reliability. On the output side, the Schottky diode (MBR), with its low forward voltage drop and fast recovery time, allows unidirectional current flow with minimal losses at high frequencies. The 150 µF capacitor filters out voltage ripples to establish a stable Vbias output. The 1k and 1R resistors are added to optimize MOSFET operating conditions, limit excessive current, and ensure load stability. In this design, limitations such as the MOSFET's thermal tolerance, the leakage inductance of the transformer, and diode losses have been considered. Additionally, components are selected for their low ESR and high-speed characteristics to ensure efficient operation with minimal losses at high frequencies.

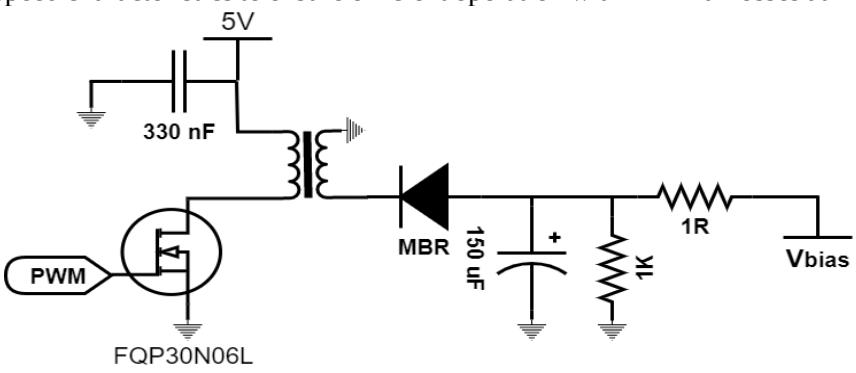

Figure 4. Reverse voltage circuit design

3. SIMULATION RESULTS AND DISCUSSIONS

LTspice v17.1.8 simulation software from Analog Devices was used to analyze the circuit comprehensively. The designed circuit consists of several stages: TIA, gain, and reverse feed. First, the reverse feed stage will be simulated, and its characteristics will be examined.

3.1. Modeling Bias Voltage

The parameters of the circuit analyzed in LTSpice are as follows:
.param D=0.15: This defines the service factor of the converter. The service factor represents the ratio of the time a cycle is “on” to the total cycle time. In this case, 15% of the cycle is set to be “on.”
.param Fs=200k: This determines the switching frequency of the converter. In this case, the converter switches at a frequency of 200 kHz.

.param Vin= 24: This determines the input voltage of the converter. In this case, the input voltage is set to 24V.

.step param X 10u 150u 10u: This command defines a parameter sweep for parameter “X.” The “X” value varies in steps of 10 microfarads (10u) from 10 microfarads (10u) to 150 microfarads (150u). This could represent a capacitor connected in parallel with the converter, and LTSpice simulates this range to see how it copes with these changes.

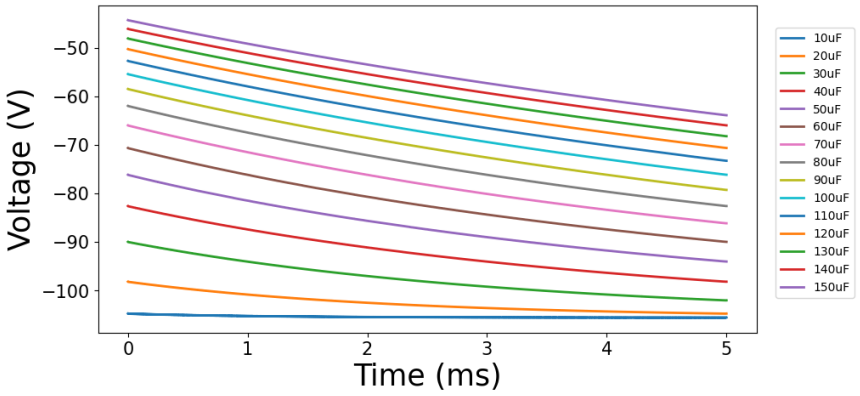

Figure 5. Flyback converter circuit PWM response.

The duty cycle (D) and switching frequency (Fs) are key parameters that must be carefully adjusted to ensure efficient operation of the flyback converter. D = 0.15 indicates that the MOSFET is on for 15% of the cycle, allowing the transformer to store and release energy without reaching magnetic saturation. If D = 0, the MOSFET never turns on, resulting in no output voltage; if D = 1, the MOSFET remains continuously on, leading to overheating and saturation in the transformer. The Fs value of 200 kHz determines how many times per second the MOSFET switches. While higher frequencies provide faster response times, they also increase heat dissipation and switching losses in the MOSFET and transformer. At lower Fs values, a higher D is possible as the transformer has more time to reset its magnetic field; however, at higher Fs values, a lower D is preferable. This combination optimizes efficiency and achieves stable output voltage. The balance between duty cycle and switching frequency is essential to manage limitations such as transformer saturation, MOSFET heating, and output voltage stability. The Vin and X parameters are critical factors that directly impact the performance and stability of the converter. With Vin set to 24V, the input voltage enables efficient operation; however, excessively high Vin values can cause overheating in components like the MOSFET and transformer, while lower Vin values may limit output power, risking insufficient voltage. The X parameter, representing capacitance connected in parallel to the output, is swept in simulation from 10 µF to 150 µF. As capacitance increases, output ripple decreases, providing a more stable output voltage; however, very high capacitance can slow the circuit's response time and lead to excessive current draw during transients. A balanced choice of these parameters is crucial for ensuring output voltage stability, fast response capability, and thermal durability of the components.

As can be seen from the graph, the response of the circuit driven by the 150 µF capacitor is ideal for TIA. When analyzing the TIA circuit, it will be assumed that the required reverse bias voltage will be given ideally.

3.2. Distance Dependent Iapd Current Modeling

The current falling on the APD varies inversely with the distance of the laser signal. In this project, a 905 nm, 30 mW, 5 V DC IR laser unit with 0-15 kHz TTL modulation (18×45 mm) is used. The 905 nm wavelength falls within the APD's maximum sensitivity range of 500-1000 nm, ensuring high efficiency. Additionally, the 30 mW laser power is sufficient to generate a high photocurrent from the APD; if the laser power were lower, the photocurrent from the APD would decrease, negatively affecting the signal-to-noise ratio, making 30 mW an optimal choice. When the laser illuminates the APD, the current passing through the photodiode depends on the laser's power, the APD's sensitivity, and gain. APDs achieve high gain by multiplying the carriers produced by each photon of incident light. This multiplication process allows currents ranging from nanoamperes to microamperes, depending on the light intensity on the device's surface.

Given the APD's responsivity value of 60 A/W and the laser's output power of 30 mW (i.e., 0.030 W), the APD's high responsivity, combined with high gain, allows even small amounts of incident light to be converted into a high photocurrent. Therefore, the APD is designed to operate with high sensitivity even at low light levels. However, at higher laser powers and gain factors, limitations such as overheating and saturation should be considered, as the APD's thermal capacity could become a limiting factor under these high-power conditions. With these values, we can calculate the current passing through the APD. With these values, we can calculate the current passing through the APD.

$$I = \text{Responsivity} \times \text{Light Power} \tag{2}$$

$$I = 60 \times 0.030 \; = \; 1.8 \text{ mA} \tag{3}$$

In this case, the current flowing through the APD will be approximately 1.8 mA. This shows how the light from the laser is detected by the APD and how much photocurrent this light produces. The distance measurement of the laser can also be made from here. To calculate how the photocurrent produced by laser light on a photodiode varies with the distance of the laser from the photodiode, we must consider the light's propagation properties and geometry. As the distance increases, the light coming from the light source decreases as its area expands. This can be explained by the fact that light intensity decreases inversely proportional to the square of the distance (inverse square law).

Calculation:

- Initial Conditions,
- Laser Power, P=30 mW
- APD Responsivity, R=60 A/W
- Current at First Distance, I=1.8 mA

Current-Distance Relationship:

- In the first case, when the laser is very close to the APD, 1.8 mA is obtained with the equation $I=R\times P$.
- As the laser moves away, the effective area of light falling on the APD decreases. As the distance increases by d units, the light intensity decreases by $1/d^2$.

New current (I_d), at distance d:

$$I_d = I + \; d^2 \tag{4}$$

Here, I is the starting current (1.8 mA), and d is the ratio of the distance of the laser from the APD to the starting distance. This analysis measures the designed circuit's response according to the laser distance. The focal point of the laser we use here is 10 cm. In other words, it is at the maximum current that the APD can see. Here, we will examine how the current through the APD (Iapd) responds to distance changes. Using the LTspice simulation, we will observe how the buffer output, that is, the circuit output, changes step by step by increasing or decreasing the distance of the laser from the APD. This analysis will help us understand the sensitivity of the APD to light sources at various distances and the long-distance sensing capability of our system. Using the ".step" command, this study will enable us to model scenarios encountered in practical applications.

```
.step param IAPD 0u 1.8m 200u
PULSE(0 {IAPD} 0 0.9n 0.9n 20n 200n)
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In the PULSE command, a PWM signal is defined, starting from 0 μA and going up to 1.8 mA. It has a rise and fall time of 0.9 ns. Additionally, PW is 20 ns, and PRI is 200 ns.

The IAPD parameter is a sweep parameter used to define the APD's output current, varying from 0 µA to 1.8 mA in steps of 200 µA. This range is tested in simulations to observe how different light intensities and gain levels affect circuit behavior under varying conditions. The upper limit of 1.8 mA is set to prevent the APD from overloading or exceeding its thermal capacity, ensuring stable operation. The PULSE command applies a PWM signal to the APD output current, starting at 0 µA and reaching up to the limit defined by IAPD. With a rise and fall time of 0.9 ns, optimized for the Excelitas C30737 APD's rapid response, this setting preserves signal integrity at high frequencies, allowing the APD to handle fast laser pulses efficiently. The pulse width (PW) of 20 ns determines the duration for which the APD signal remains at its peak, suitable for applications requiring quick response. The period (PRI) of 200 ns sets the signal repetition rate, producing a new pulse every 200 ns, which enables the APD to process high-speed incoming signals and maintain the characteristics of the laser pulse in the output. Together, these parameters are optimized to allow the APD to operate effectively under different light conditions and high-speed scenarios, although considerations like thermal noise and heating at high frequencies may impose limitations on performance.

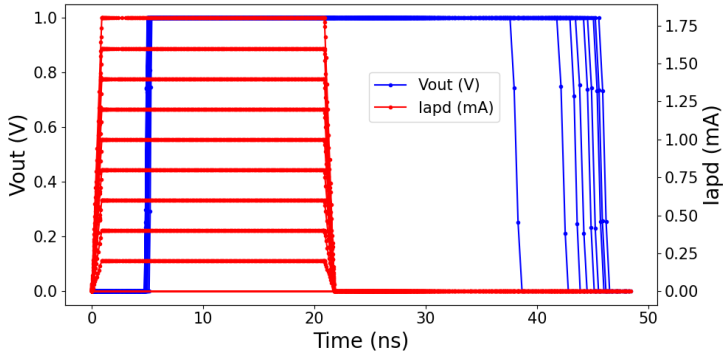

Figure 6. Relationship between 22 ns PW and laser distance

The graph in Figure 6 shows the current coming to the APD according to the laser distance and, accordingly, the voltage in the buffer at the output of the circuit. It is observed that when a 22 ns PW signal is sent, the current takes different values, and therefore, the output voltage in the buffer changes. The blue line shows the voltage (V) and progresses at a constant value on the time (ns) axis. The red line shows the current (mA) and fluctuates at different levels on the time axis. It is observed that the current takes different values and changes in direct proportion to the distance of the laser. As the current increases (for example, as the laser approaches the APD), the current value increases and vice versa. While the output voltage at the buffer is expected to remain at a constant value when a 22 ns PW signal is sent, it sometimes varies for longer or shorter periods than this period. This is due to the circuit's response to different current levels.

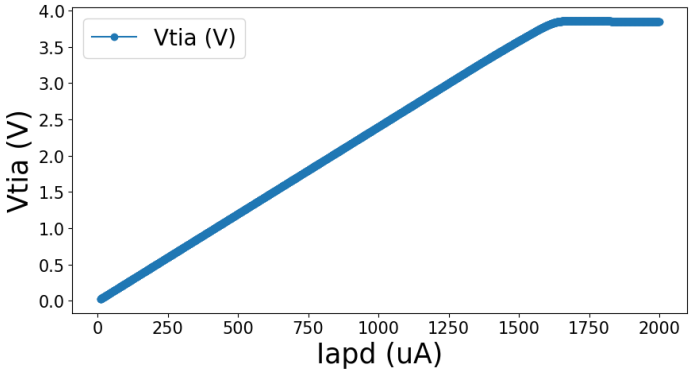

Figure 7. Iapd response of the TIA

As the distance of the laser from the APD increases, the current value decreases, and as the distance decreases, the current value increases. The initial current is given as 1.8 mA, and the graph shows that the current varies at different distances. The change in current directly affects the output voltage in the buffer. More significant fluctuations in the output voltage are observed, especially at higher current values (when the laser is close to the APD). This shows that the circuit's responses to current levels differ and cannot provide a constant output voltage against these changes. If we do the DC analysis of Iapd,

.dc Iapd 0 2m 10u

The .dc Iapd 0 2m 10u command is used to perform a DC analysis of the APD current (Iapd). This command varies the Iapd value from 0 µA to 2 mA in 10 µA steps. This range is chosen to simulate the intensity of laser light received by the APD at different distances and to understand how current variations affect the output voltage. The 0 µA starting value represents a scenario where the laser light does not reach the APD or is very distant, while the 2 mA upper limit approximates the maximum detection range of the APD, simulating the highest current level when the laser is very close to the APD. This upper limit is also chosen to be close to the ±2 mA input current limit of the LTC6268 op-amp, ensuring the stability and safety of the op-amp. The 10 µA step analysis allows for capturing fine details of the relationship between the distance of the laser to the APD, the resulting current, and the output voltage, particularly observing how the circuit responds to higher current values (closer distances). This DC sweep analysis provides a detailed evaluation of how current changes affect the circuit's voltage output, revealing the circuit's capability to maintain a stable voltage under varying light conditions.

In the graph in Figure 7, as the input current, that is, the current passing through APD, increases, the output voltage of the TIA circuit reaches DC saturation. After 1.7 mA, the output voltage settles at 3.7 V. This coincides with the characteristics of APD. The maximum current passed by the APD is calculated as 1.8 mA and is related to the power of the pulsed laser. According to the analysis, APD saturates at small distances and focal points from the focal point of APD. Therefore, in such cases, PW measurement is performed incorrectly.

3.3. PW and PRI Analysis

PW is the duration of the laser pulse and is usually measured in nanoseconds or microseconds. Pulse width affects the pulse's energy and, therefore, its level of detectability. Pulse width can directly affect data transmission speed and resolution. PRF refers to the number of pulses sent in one second, measured in Hz. PRF determines the system capacity and data transmission rate. High PRF provides fast data transmission but is limited to shorter sensing distances because the inter-pulse time is shortened. PRI is the time interval between two consecutive laser pulses. PRI helps determine the detection distance and speed of the target defined by the system. When long distances need to be detected, longer PRI values are generally used.

In optical communications, especially in applications such as LIDAR, these parameters determine how quickly and effectively laser pulses can detect targets and data transmission efficiency. For example, faster scanning can be done in a LIDAR system using high PRF, which is advantageous in rapidly changing conditions such as moving vehicles. However, higher PRF may result in shorter-range detection because the system may not receive a response quickly enough before sending the next pulse. Conversely, long PRI allows the detection of greater distances but reduces the speed of data collection. Therefore, setting these parameters appropriately depending on the system requirements is critical. Balanced optimization of these parameters in pulse laser systems in optical communication is essential for maximum efficiency and performance.

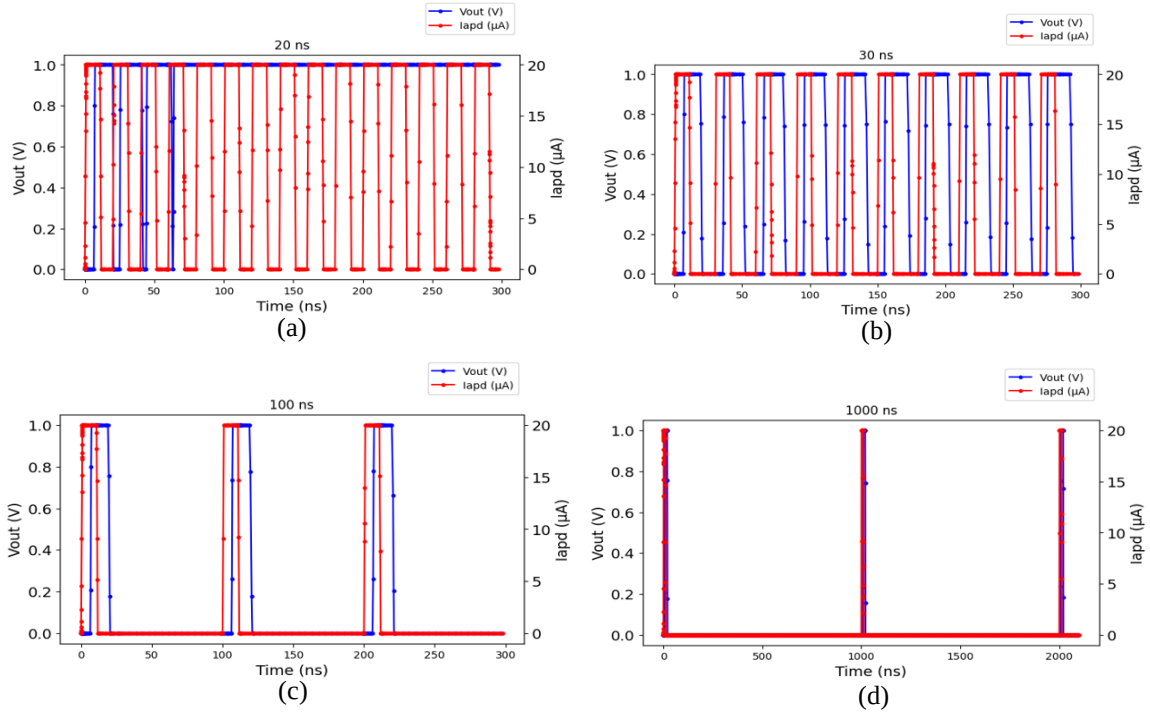

Figure 8. Pulse reputation interval, (a) 20; (b) 30; (c) 100; (d) 1000 ns

The PULSE command parameters, PW (Pulse Width) and PRI (Period), were carefully selected to determine the stable and unstable operating limits of the TIA circuit. The PW value is set to 10 ns, which is suitable for high-speed applications where the TIA circuit needs to detect laser signals quickly. However, if the PW value is too short, it may hinder the signal processing by not allowing enough energy to accumulate within the circuit. The PRI value, on the other hand, allows the circuit to complete its energy processing and prepare for the next pulse. By using different PRI values, such as 20 ns, 30 ns, 100 ns, and 1000 ns, a range was established in which the TIA circuit shows instability at lower PRI values and stability at higher ones. At a PRI of 20 ns, distortions in the output signal were observed due to insufficient time for the circuit to stabilize, whereas a PRI of 30 ns resulted in more regular and periodic pulses. With longer PRI values of 100 ns and 1000 ns, the circuit produced completely stable and smooth outputs, with the 1000 ns PRI delivering the most consistent and stable signals. These results reveal that the TIA circuit exhibits instability at short PRI durations but provides reliable performance at higher PRI values. Therefore, the PULSE command parameters were chosen to cover a broad range, from the lower PRI values, where the circuit shows instability, to the higher PRI values, where it produces stable results. This selection established an operational frame within which the circuit can maintain a stable output voltage.

The ".step param PW 5n 155n 50n" command was used to analyze the response of the TIA circuit based on varying pulse width (PW) values. In each simulation step, the PW parameter is set to 5 ns, 50 ns, and 155 ns to observe how the circuit behaves across different operating conditions. The 5 ns PW value represents a very short pulse width, chosen to test the circuit's response under high-speed conditions where signal processing time is limited. At this low PW, the circuit may not have sufficient time to accumulate and process energy, potentially leading to output distortions. The 50 ns PW is an intermediate value that provides a more stable operation, allowing the circuit adequate time for signal processing and reducing output irregularities. This setting represents a transition point between unstable and stable operation. The 155 ns PW represents a high pulse width, giving the circuit ample time to process the signal and produce the most stable and accurate output. This range of PW values, spanning

from 5 ns to 155 ns, was selected to cover the frame in which the TIA circuit transitions from unstable to stable operation, thereby identifying the conditions under which the circuit provides the most reliable output. Through this analysis, the optimal PW range for stable voltage output and the limits of instability at shorter PW values were determined.

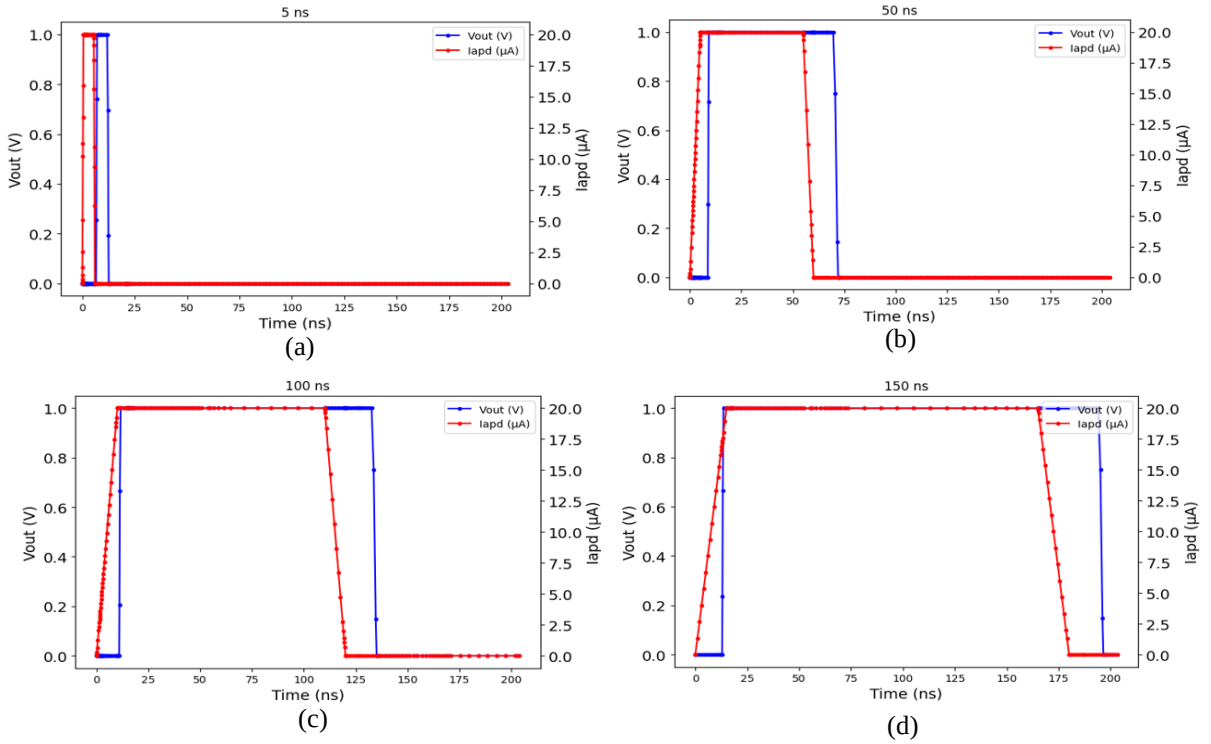

Figure 9. Pulse width, (a) 5; (b) 50; (c) 100; (d) 150 ns

Figure 9 shows the effects of the circuit on the output voltage (Vout) and the current from the APD (Iapd) when the PW parameter is set to 5, 50, 100, and 150 ns. The blue lines in the graphs represent Vout, and the red lines represent Iapd. At 5 ns PW (upper left graph), Vout rises and falls rapidly, and Iapd synchronously exhibits the same behavior without any degradation, indicating a fast circuit response. At 50 ns PW (upper right graph), Vout produces a longer pulse, and Iapd works accordingly correctly. At 100 ns PW (bottom left graph), the Vout signal remains high for more extended and Iapd again rises and falls in line with Vout. At 150 ns PW (bottom right graph), Vout generates the longest pulse width, and even then, the Iapd signal operates smoothly without significant degradation. This analysis allows us to observe the circuit's response at different values of the PW parameter. It shows that the output voltage (Vout) and the current (Iapd) signals from the APD are compatible and stable at each pulse width. As a result, the TIA circuit exhibits stable performance at various pulse widths. It works appropriately even at high frequencies, proving that it is designed to meet high-performance requirements in optoelectronic applications.

3.4. Dark Current Modeling and Analysis

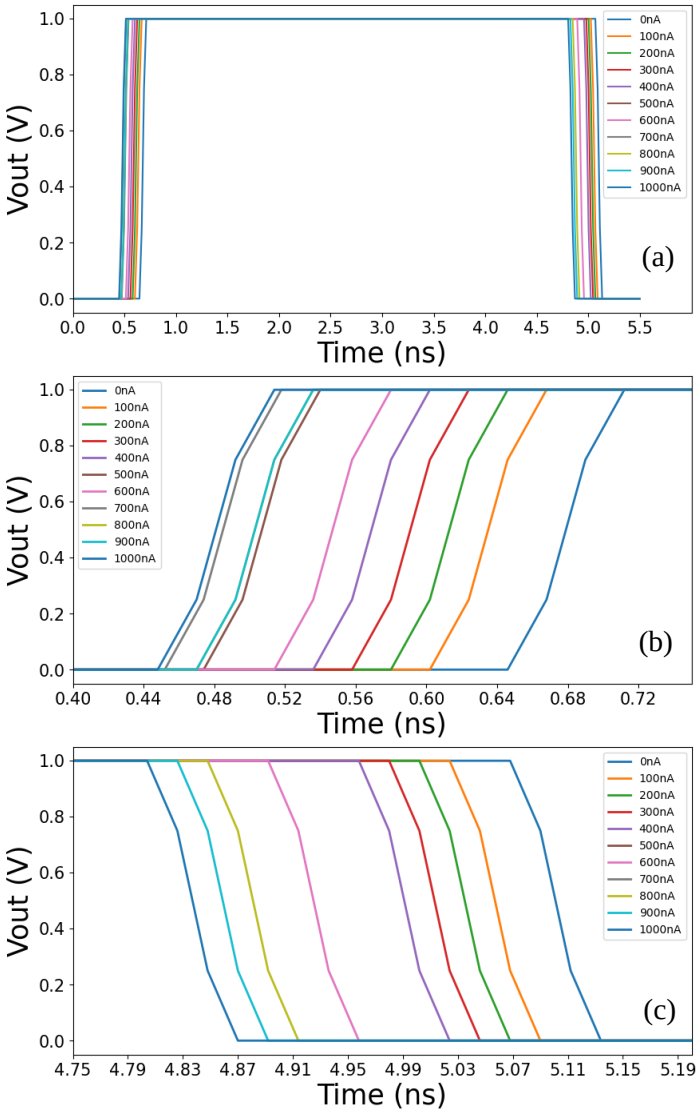

Figure 10. Dark current analysis of the APD, (a) full scale; (b) around 0.5 ns; (c) around 5 ns

The effects of the amount of dark current on the performance of the APD and TIA circuit will be examined in this section. We will analyze the circuit's reaction to these changes by changing the dark current value with the ".step" command on LTspice. Control of dark current is essential to minimize noise and maximize signal integrity, especially at low signal levels. Dark current values range from nanoampere, nA to microampere, µA. Especially in APDs designed for low-light applications, dark current values are tried to be kept lower. Typically, in silicon-based APDs, dark current values can range from a few nA up to 100 nA. However, these values can increase to microamperes at high gain settings or temperatures. The step command sets dark current values between 0 nA and 1000 nA to observe the performance of the APD circuit under both low and high dark current conditions. Dark current in APDs typically ranges from as low as 0.05 nA up to several µA; therefore, a broad range from 0 nA to 1000 nA is included in the simulation. Low dark current values are chosen to test the APD's sensitivity for precise signal detection, while higher values allow examination of potential reductions in signal

sensitivity and possible noise increases. This range provides an operational framework in which the circuit responds with stability and sensitivity at lower levels, while stability is tested at higher levels.

Figure 10 shows the response of the APD and TIA circuits with various dark current values on the time (ns) and voltage (V) axes. The graph shows the voltage changes for different dark current levels (0, 100, 200…,1000 nA). The effect of different dark current levels is observed in the graph. Each colored line represents a specific level of dark current. Voltage values increase and decrease quickly, showing that the circuit responds quickly. The time axis is in ns, indicating that responses occur quickly. As dark current values increase, very slight differences are observed in the voltage curves. While voltage changes are more noticeable, especially at low levels, these changes become less evident at high levels. As dark current levels increase, a slight deviation in the voltage response of the APD and TIA circuits is observed. This shows that dark current can affect the overall performance of the circuit. The circuit's response is quite sensitive for low dark current levels (e.g., between 0nA and 100nA), and a significant voltage change is observed. This highlights the importance of keeping dark current to a minimum at low signal levels. At higher levels (e.g., 900 to 1000 nA), less pronounced changes in voltage response are observed. This suggests that high dark current levels can reduce the circuit's sensitivity and potentially increase noise levels.

3.5. Bode Diagrams of The Circuit

Bode diagrams were generated to analyze the frequency response of various circuit layers. This analysis shows the effect of filter circuits and gain stages throughout the system and their frequency-dependent behavior. Bode diagrams are an excellent tool for understanding frequency-dependent changes critical in circuit design.

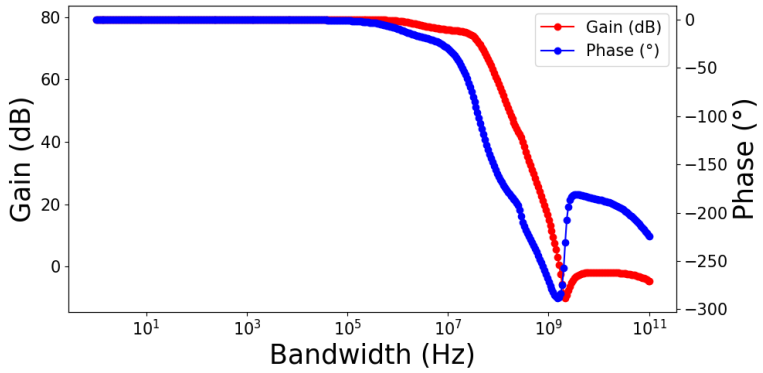

Figure 11. TIA with T-network AC analysis gain and phase graph

Figure 11 shows the gain in dB versus frequency for a TIA equipped with a T-network. In this graph, the gain curve is represented in red. This analysis is essential to understanding the T-network's effect on the TIA circuit's gain performance in different frequency ranges. In the low-frequency region (10 Hz-1 kHz), the gain remains constant at approximately 80 dB. There is no significant change in gain as the frequency increases. This shows that the TIA circuit provides a high and stable gain at low frequencies. In the mid-frequency region (1 kHz-10 MHz), the gain remains constant at approximately 80 dB. There is no decrease in earnings in this range either. It appears that the T-network preserves the gain of the TIA circuit in this frequency range. In the high-frequency region (10 MHz-1 GHz), the gain drops dramatically to 0 dB; after 1 GHz, the gain decreases further. The observed decrease in gain indicates that the performance of the TIA circuit decreases rapidly at very high frequencies. The gain decreases rapidly in the high-frequency region (1 GHz and above), dropping to approximately -10 dB and approaching 0 dB again. It is understood that the TIA circuit has difficulty providing gain in this frequency range, and its performance decreases significantly. However, this decay curve in the graph

shows that the T-network does not entirely lose the gain, or very little, even at very high frequencies, providing an increase of approximately 0 dB.

Figure 11 also shows the change in phase angle versus frequency for a TIA equipped with a T-network. In this graph, the phase curve is represented in blue. This analysis is essential to understand the T-network's effect on the TIA circuit's phase response in different frequency ranges. In the low-frequency region (10 Hz-1 kHz), the phase angle remains constant at approximately 0 degrees. This shows that the TIA circuit can effectively control the signal phase at low frequencies. In the mid-frequency region (1 kHz-10 MHz), the phase angle remains constant at approximately 0 degrees. No phase shift is observed in this range. It appears that the T-network maintains the phase performance of the TIA circuit in this frequency range. The phase angle decreases in the high-frequency region (10 MHz-1 GHz). A negative shift in phase angle is observed in this range. After 1 GHz frequency, the decrease in phase angle becomes more pronounced and decreases to approximately -280 degrees. This suggests that the TIA circuit has difficulty controlling the signal phase at high frequencies. When we look at the phase angle movements in the very high-frequency region (1 GHz and above), it increases rapidly up to -180 degrees. Then, it decreases quickly to approximately -250 degrees at 100 GHz. In this frequency range, the phase shift of the TIA circuit increases significantly. However, this curve in the graph shows that the T-network can partially control the phase shift even at very high frequencies.

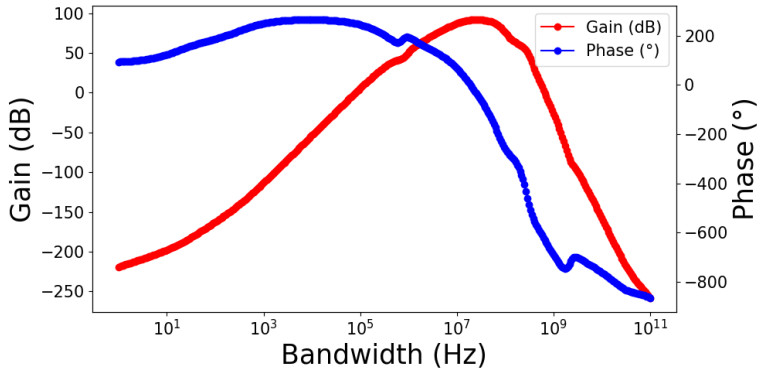

Figure 12. Gain and phase graph of the gain part of the circuit

Figure 12 shows the gain versus frequency of a gain stage in dB. In this graph, the gain curve is represented in red. This graph helps us understand how the circuit performs in different frequency ranges. The gain is meager in the low-frequency region (10 Hz-1 kHz), starting from approximately -200 dB. As the frequency increases, the gain rises slowly. This shows that the circuit cannot provide sufficient gain at low frequencies. The gain increases significantly in the mid-frequency region (1 kHz-10 MHz). In this frequency range, the gain characteristic of the TIA progresses towards optimum signal processing capability. In this region, the circuit's performance improves significantly. The 10 MHz-100 MHz frequency region, the gain reaches its peak and maximum level. The maximum gain is approximately 100 dB. This shows that the circuit provides the highest performance in this frequency range. It appears that it is in this frequency range that it can process signals most efficiently. The gain decreases again in the frequency region of 100 MHz and above. As the frequency increases further, the gain decreases. This means the circuit's performance decreases at very high frequencies and has difficulty providing gain.

Figure 12 also shows the change in the phase angle of a gain stage versus frequency. In this graph, the phase curve is represented in blue. This analysis is essential to understand the phase response of the circuit in different frequency ranges. The phase angle starts at a positive value in the low-frequency region (10 Hz-1 kHz) and increases slowly. As the frequency increases, small increases in phase angle are observed. This shows that the circuit can control the signal phase at low frequencies. The change in

phase angle becomes more evident in the mid-frequency region (1 kHz-10 MHz). The phase angle reaches a maximum of approximately 200 degrees. In this range, the circuit appears to follow the signal phase adequately, and the phase shift is relatively under control. The phase angle decreases to negative values in the high-frequency region (10 MHz-10 GHz). The decrease in phase angle indicates that the circuit has difficulty controlling the signal phase at high frequencies. In this region, the phase shift becomes evident and decreases to approximately -750 degrees. In the high-frequency region (10 GHz and above), the phase angle decreases rapidly and drops to approximately -800 degrees. This shows that at very high frequencies, the phase shift of the circuit is very severe and cannot correctly follow the signal phase.

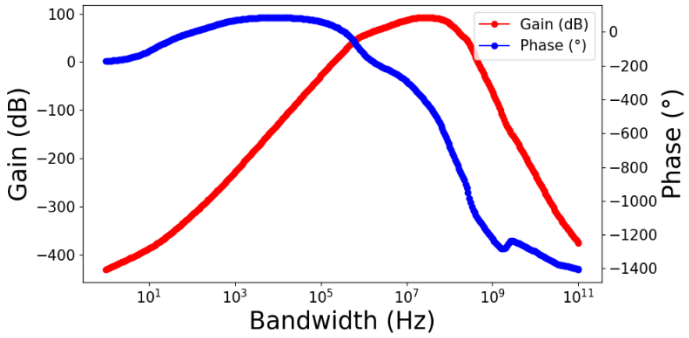

Figure 13. Gain and phase graph of the comparator part of the circuit

Figure 13 shows the gain of a comparator circuit output versus frequency in dB. In this graph, the gain curve is represented in red. This analysis is essential to understand the gain performance of the circuit in different frequency ranges. The gain is meager in the low-frequency region (10 Hz-1 kHz), starting from approximately -400 dB. As the frequency increases, the gain rises slowly. This shows that the comparator circuit output cannot provide sufficient gain at low frequencies. The gain increases significantly in the mid-frequency region (1 kHz-1 MHz). In this frequency range, the gain rises to approximately 50 dB. In this range, the comparator circuit output appears to reach its optimum signal processing capacity. The gain reaches its peak and maximum level in the 1-100 MHz frequency region. The maximum gain is approximately 100 dB. This shows that the circuit provides the highest performance in this frequency range. It is understood that in this frequency range, the comparator circuit output can process the signals most efficiently. The gain decreases again in the frequency region of 100 MHz and above. As the frequency increases further, the gain decreases. This means the circuit's performance decreases at very high frequencies and has difficulty providing gain.

Figure 13 also shows the change in the phase angle of a comparator circuit output against frequency. In this graph, the phase curve is represented in blue. This analysis is essential to understand the phase response of the TIA circuit at different frequency ranges. The phase angle starts at a negative value in the low-frequency region (10 Hz-1 kHz) and decreases slowly. As the frequency increases, small changes in the phase angle are observed. This shows that the circuit can control the signal phase at low frequencies. The change in phase angle becomes more evident in the mid-frequency region (1 kHz-10 MHz). The phase angle increases to approximately 0 degrees. In this range, the comparator circuit output follows the signal phase properly, and the phase shift is relatively under control. In the high-frequency region (10 MHz-10 GHz), the phase angle decreases again and drops to negative values. The decrease in phase angle indicates that the circuit has difficulty controlling the signal phase at high frequencies. In this region, the phase shift becomes evident and decreases to approximately -1300 degrees. The phase angle decreases rapidly in the high-frequency region (10 GHz and above) and drops to approximately -1400 degrees. This shows that at very high frequencies, the phase shift of the comparator circuit output is very severe and cannot correctly follow the signal phase.

3.6. Modeling and Analysis of Noise

In this analysis, different noise divider (ND) values were chosen to observe the impact of noise on circuit performance. These values were incrementally reduced from high noise levels to low noise levels, creating a framework that spans from erroneous circuit responses to stable performance. ND values of 5000, 7000, 9000, and 10000 were selected, and measurements were taken at these levels. These values were chosen to understand how noise affects the circuit, at which levels it adversely impacts performance, and where acceptable results are achieved. High ND values (such as 100000) were used to minimize the effects of noise and observe the circuit's performance under ideal conditions. To analyze the impact of noise on the circuit, white noise at 2 terahertz was applied and scaled by a specific factor. This design framework aims to assess the circuit's sensitivity to both low and high noise levels, thereby evaluating the effectiveness of suitable noise reduction techniques.

In the last heading, we will examine the effects of the noise added to the system on the output of the circuit depending on distance changes. This analysis will enable us to model the impact of possible noise sources on circuit performance in real-world conditions and evaluate the effectiveness of various noise reduction techniques. In this study, which we carried out using LTspice, we examined the noise effects on the circuit's input current and output voltage under various white noise intensity values. The PRI value was kept constant using the pulse signal created with the "PULSE(0 20u 0 0.9n 0.9n 10n 40n)" command. To add noise, the expression "V = (white(2e12 * time) / ND)" was used, and noise divider (ND) values were determined as 5000, 7000, 9000, and 10000, and measurements were taken for these values. White noise was at a frequency of 2 terahertz and was added to the current source by scaling with different noise divider values. Mathematically, the standard deviation of this noise is calculated by multiplying the power density of the white noise by time and scaling by a particular factor.

$$\sigma_{\text{noise}} = \sqrt{\text{PSD} \times \Delta f \times t} \tag{5}$$

$$\sigma_{\text{noise}} = \frac{1}{\text{GB}} \times \sqrt{2 \times 10^{12} \times t} \tag{6}$$

In Equation (5) above, PSD is the power spectral density, and Δf is the frequency bandwidth. σ_{noise} is the standard deviation of the noise. For noise divider values, the standard deviations of white noise at a given time were calculated in Table 1.

Table 1. Standard deviation values according to ND (noise divider) values

ND	σ_{noise}
5000	282.8
7000	202.0
9000	157.1
10000	141.4
20000	70.7
30000	47.1
40000	35.4
100000	14.1

These calculations show the standard deviation of white noise at a specific time instant (1 second). As can be seen, as the noise divider value increases, the standard deviation of white noise decreases, and the noise effect remains at lower levels. This provides more regular and stable results at high noise divider values. Additionally, an analysis was made according to these ND values, and the results were observed. LTspice commands used:

PULSE(0 20u 0 0.9n 0.9n 10n 40n) generates a pulse signal with a peak value of 20 μA. PW is 10 ns, and the period is 40 ns.

V = (white(2e12 * time) / ND), adds white noise. The expression "white(2e12 * time)" creates white noise at a frequency of 2 terahertz, and the ND value scales this noise.

I = I(Iapd) + V(NOISE) adds white noise to the stream from the APD. The expression represents the noise voltage V(NOISE).

As seen in Figure 14, severe distortions were observed at the output of the circuit at low noise divider values (5000 and 7000), and the desired smooth pulses could not be obtained. Voltage and current graphs are irregular and highly affected by noise. The output showed more regular and periodic pulses at higher noise divider values (9000 and 10000), but there was still a significant noise effect. It continued to show more regular and periodic pulses at the noise divider values of 20000 and 30000, but a completely clean output signal could not be obtained. Likewise, voltage and current graphs are irregular and highly affected by noise. When we further increase the noise divider values (40000 and 100000), we finally see that the output signal shows more regular and periodic pulses. These results show that the circuit does not show the desired performance at low noise divider values, and severe distortions occur. However, more stable and smooth results are obtained at high noise divider values. The output signal exhibits more regular and periodic pulses at the noise divider values of 40000 and 100000. This indicates that higher noise divider values significantly improve the circuit's performance, reducing the impact of white noise. With the addition of white noise, changes in the system's performance became more evident, and the sensitivity of the TIA circuit to noise was analyzed. This analysis highlights the need to consider noise effects when designing and implementing the TIA circuit to achieve optimal performance.

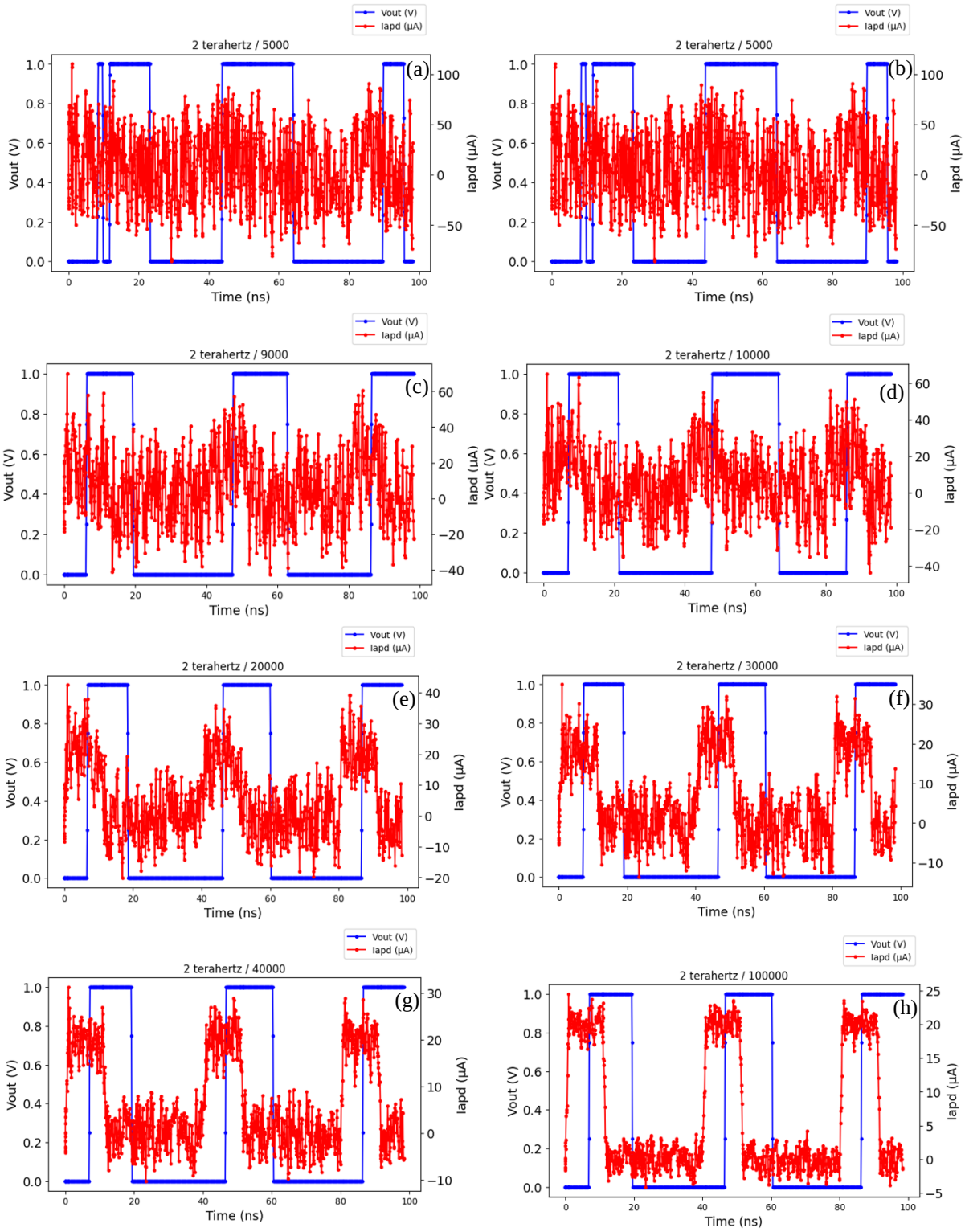

Figure 14. TIA's white noise response, (a) 2 THz/5000; (b) 2 THz/7000; (c) 2 THz/9000; (d) 2 THz/10000; (e) 2 THz/20000; (f) 2 THz/30000; (g) 2 THz/40000; (h) 2 THz/100000.

3.7. Feedback Capacitor Analysis

In this section, the reactions of the circuit output according to the values of the feedback capacitor in the TIA circuit have been analyzed. This analysis was performed using the .step param TC 1p 5p 1p command. In this analysis, different feedback capacitor values in the TIA circuit were used to observe their effects on the circuit output. The ".step param TC 1p 5p 1p" command was employed to vary the capacitor value between 1 pF and 5 pF in 1 pF steps, allowing for an analysis of the circuit's response. These values were chosen to examine how the TIA circuit responds across a range of low to high capacitance levels. Low capacitor values provide a faster response time but may reduce output stability, while higher capacitor values make the circuit more stable but slow down its response time. Thus, the feedback capacitor values were selected within a broad range to identify the stable and unstable operating limits of the circuit. This framework enables the determination of optimal feedback capacitance values for achieving the best output performance in the circuit.

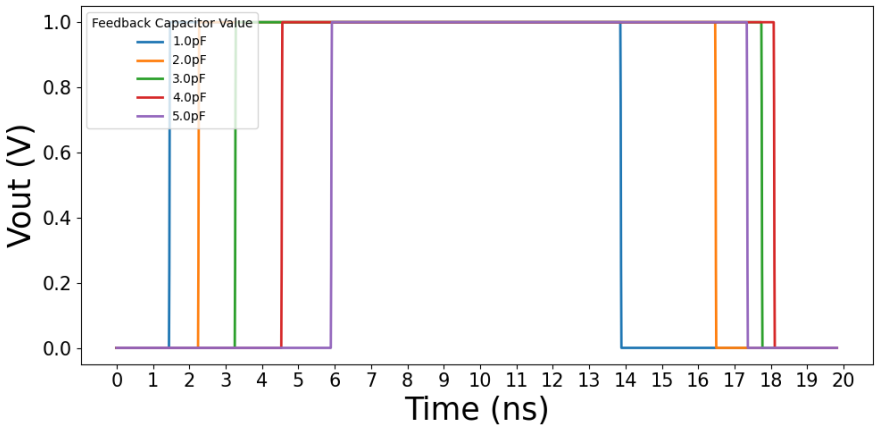

Figure 15. T-network capacitor response

Within the feedback capacitor analysis scope, the feedback capacitor's value in the T-network was calculated parametrically, and the input and output pulse widths (PW) were examined using these values. The colored lines in the graph in Figure 15 show the voltage changes corresponding to each capacitor value. These results demonstrate how the feedback capacitor value affects the pulse width and, thus, the system performance. The graph shows voltage changes on the time axis for different feedback capacitor values (1.0 pF, 2.0 pF, 3.0 pF, 4.0 pF, and 5.0 pF). It was observed how the pulse width changed for each capacitor value. According to the analysis results, narrower output pulses are obtained with lower feedback capacitor values (1 pF), while the output pulse width increases with higher capacitor values (5 pF). This shows that optimizing the feedback capacitor value is critical for system performance. By selecting the appropriate value of the feedback capacitor, the TIA circuit can achieve the desired performance. This study highlights the effect of feedback capacitor value on pulse width and provides an essential basis for determining the optimal capacitor value. This analysis applied a 0.9 ns rise, 0.9 ns fall, and a 10 ns wide pulse to the input, resulting in a total PW of 12 ns. In this case, a 12 ns pulse width at the output was provided with a 1 pF feedback capacitor, and the suitability of this capacitor for the circuit was measured.

The capacity of the TIA circuit to convert weak signals from APDs into electrical signals with high accuracy has been successfully demonstrated. A high-performance TIA circuit is designed for optical communication and sensing systems, providing wide bandwidth, high gain, and low noise performance. It has been observed that the circuit can produce stable and regular pulses at high PRI values. At low PRI values, serious deteriorations in circuit performance were observed, and the desired smooth pulses

could not be obtained. It has been determined that at low noise divider values, the performance of the circuit is negatively affected by the noise effect, and the output signals are irregular. It has been found that optimization of the feedback capacitor plays a critical role in pulse width and system performance.

The developed TIA circuit offers promising results for high-performance optical communication and sensing systems applications. This circuit seems to be used primarily in applications requiring high sensitivity, low noise, and wide bandwidth. Optimizing and testing the design in various real-world conditions will provide an essential basis for future research. The findings of this study provide vital information for the development of optical communication and detection systems and contribute to technological advances in this field. In the design and applications of the TIA circuit, parameters such as optimization of the feedback capacitor value, effects of white noise, and correct selection of PRI values are critical. These findings provide a promising roadmap for developing high-performance TIA circuits in optoelectronic systems. Future studies may further improve the performance of the TIA circuit by examining and optimizing these parameters in more detail and enabling its integration into broad application areas.

4. CONCLUSION

The bias voltage was modeled using a flyback converter circuit in LTSpice with the following parameters: duty cycle of 15%, switching frequency of 200 kHz, and input voltage of 24 V. The circuit's response driven by a 150 μF capacitor was ideal for the TIA circuit. The current through the APD was modeled based on the distance of the laser signal. Using a responsivity value of 60 A/W and a laser power of 30 mW, the current was calculated to be 1.8 mA. The current decreased with increasing distance according to the inverse square law. The effects of pulse width (PW) and pulse repetition interval (PRI) on the circuit's output were analyzed. Measurements were taken for PRI values of 20, 30, 100, and 1000 ns. More stable pulses were observed at higher PRI values. The pulse widths analyzed were 5, 50, 100, and 150 ns, showing stable performance at all values. The effect of dark current on the APD and TIA circuit was examined by varying the dark current values from 0 to 1000 nA. Voltage changes were more noticeable at lower dark current levels, indicating the circuit's sensitivity to dark current. The gain and phase response of the TIA circuit with a T-network was analyzed using Bode diagrams. The gain remained constant at approximately 80 dB from 10 Hz to 10 MHz but decreased significantly at higher frequencies. The phase response remained steady at approximately 0 degrees from 10 Hz to 10 MHz, then decreased to -280 degrees at 1 GHz and to -250 degrees at 100 GHz. The impact of white noise on the circuit's performance was analyzed by adding noise with different noise divider values of 5000, 7000, 9000, 10000, 20000, 30000, 40000, and 100000. Higher noise divider values resulted in more stable and periodic pulses, reducing the noise effect on the circuit. The value of the feedback capacitor in the TIA circuit varied from 1 pF to 5 pF to analyze its effect on the pulse width and system performance. Lower feedback capacitor values resulted in narrower output pulses, while higher values increased the pulse width. This showed the importance of optimizing the feedback capacitor value for system performance.

CONFLICT OF INTEREST

The authors stated that there are no conflicts of interest regarding the publication of this article.

AUTHORSHIP CONTRIBUTIONS

Berkay ÇAVUŞ: Circuit Modeling, Circuit Design, Methodology, Visualization, Writing – original draft. **Şekip Esat HAYBER:** Supervision, Writing – review & editing.

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