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*Research Article*

# Design and implementation of the FPGA-based chaotic van der pol oscillator

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ABSTRACT

In this study, the chaotic Van der Pol system was implemented for real-time chaos applications on FPGA chip. The chaotic Van der Pol system was also modelled numerically by using the Euler algorithm ODE (Ordinary Differential Equation) solver on Matlab. Numerical structure of the chaotic Van der Pol oscillator designed on Matlab was taken as reference for the design of FPGA-based chaotic Van der Pol oscillator unit. The chaotic Van der Pol system was coded in Very High-Speed Integrated Circuits Hardware Description Language (VHDL) with 32-bit IEEE-754-1985 floating point number standard. The designed chaotic Van der Pol system was synthesized in the Xilinx ISE Project Navigator program and was implemented on the Xilinx VIRTEX-6 chip family, XC6VLX75T device, FF784 package. The maximum operating frequency of the FPGA-based chaotic Van der Pol oscillator unit obtained from Place and Route processes was 498.728 MHz. Additionally, chip statistics of the FPGA-based Van der Pol oscillator were presented.



## 1. Introduction

Chaos or chaotic systems are one of the fields theorized in recent years and studied extensively. Some of the research areas related to chaos or chaotic systems are oscillator design [1], biomedical [2], communication [3], optical [4], power electronics [5], robotic [6], artificial neural networks [7-9], pseudo random number generator [10], true random number generator [11], synchronization [12], image processing [13], optimization [14]. Chaotic oscillators are used in many applications because of their characteristic features, such as the fact that signals generated by them show noise-related and non-periodic behaviors, and they depend on the initial conditions and the system parameters very sensitively. Therefore, many chaotic systems with different characteristics are proposed in the literature. From these chaotic systems, the oscillators, whose system dynamics are best known, are Lorenz [15], Chua [16], Shimizu-Morioka [17], Duffing systems [18], and Chen [19]. In addition, there are some other chaotic systems presented to the literature newly with their different characteristic features. [20-22]. Chaotic oscillators can be examined in two types: continuous-time and discrete-time chaotic oscillators. For the purpose of performing discrete-time chaotic oscillators, various hardware platforms such as digital Signal processors (DSPs) [23], Application Specific Integrated Circuits (ASICs) [24], microcontroller (μC) [25], and Field Programmable Gate Arrays (FPGAs) [26] are used. FPGA chips, which are one of the digital-based platforms, are frequently used in the literature because of their characteristics such as parallel processing and ability to be programmed repeatedly.

In the study conducted by Rajagopal et al., by using the RK5-Butcher algorithm and 32-bit IEEE-754 floating point standard, a new 3D chaotic chameleon system application on the Xilinx Virtex-6 XC6VLX240T FPGA chip was carried out [27]. In the study of Alçın et al., by using ANN structure and 32-bit IEEE-754 floating point standard, Pehlivan Uyaroglu Chaotic System on the Xilinx Virtex-6 FPGA chip was designed as hardware [8]. In another study, by using Heun algorithm and floating-point number format, on the Xilinx virtex-6

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FPGA chip, design and implementation of a new 3D chaotic system with a single equilibrium point was carried out by Tuna et al. [1]. In another study, Azzaz et al. modelled the 3D hybrid chaotic system with the Virtex-II family FPGA chip of Xilinx Company in accordance with 32-bit IQ-Math format, and by using this system, they carried out an application [28]. In the study of Lai et al., using the fourth degree Runge Kutta algorithm, a multi-butterfly chaotic attractor was designed with the 32-bit IEEE-754 number standard and the Xilinx Kintex-7 FPGA chip, and engineering applications were performed by using the oscillator [29]. In the study conducted by Tlelo-Cuautle and his colleagues, the chaotic system was modelled on the Altera Cyclone IV FPGA chip by using the 32-bit fixed-point number standard. [30]. Using the RK-4 algorithm and the 32-bit IEEE-754 number Standard, the Chen Chaotic System was carried out on the Xilinx virtex-II FPGA chip in real time by Sadoudi et al. [31]. Rajagopal et al. modelled the 3D Time-Delayed Chameleon Chaotic System on the Xilinx Virtex-7 XC7-VX980tffg FPGA chip by using Matlab Xilinx system generator [32].

In the second section of this study, brief information about chaotic systems, Van der Pol oscillator, FPGA chips and numerical algorithms will be given. In the third section, the design of FPGA-based Van der Pol oscillator unit will be presented. In addition, FPGA chip statistics and simulation results obtained from the design testing will be given. In the last section, the results of the study will be interpreted.

## 2. Background Information

### *2.1 Chaotic Systems and Van der Pol Oscillator*

The term Chaos was first introduced by M.I.T. scientist Edward Lorentz's work in 1963. Lorentz wanted to round down the results of the mathematical meteorological model he created with the aim of forecasting the weather, but could not get the results he wanted. In this way, the first foundations of Chaos Science Field were laid. As a definition, chaotic systems or chaos can be expressed as dynamic systems which are deterministic, non-linear, non-periodic and highly sensitive to system parameters and system startup conditions [11].

Chaotic systems are expressed by using ordinary differential equations. In the literature, there are 1st degree discrete-time chaotic systems. On the other hand, in continuous-time chaotic systems, at least a second-order differential equation set should be used. In the Equation 1, the differential equation for Van der Pol system is given. [33].

$$\frac{d^2x}{dt^2} - \mu(1-x^2)\frac{dx}{dt} + x = 0 \qquad (1)$$

The Van der Pol oscillator shows chaotic oscillator characteristics under certain conditions. In this study, while the system parameter was taken as $\mu$=0.5, the initial conditions were taken as $x_0$=1.0 and $u_0$=-0.97.

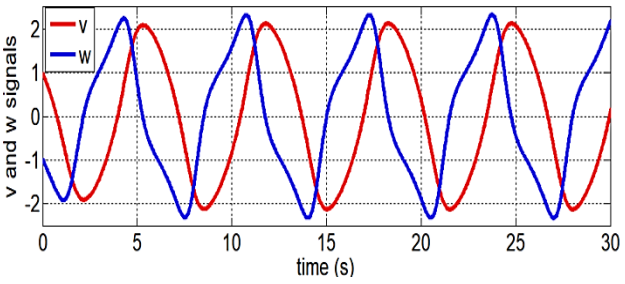


Figure 1. Time Series of the Van der Pol oscillator

### *2.2 FPGA Chips*

FPGA chips can be defined as integrated circuit tools with repeatedly programmable properties for digital system/circuit designs. These chips, after the first silicon production process, allows the designer to make system design in the chip whenever he/she wants [34]. These chips are also called as “System On a Chip” (SOC), and they can work together with other hardware platforms as part of the larger designs when needed [35]. In recent years, FPGA chips have gained quite high capacity and high performance, but their structures have become more complex day by day. FPGA chips, which are produced for general purpose and can be programmed specifically for design, have approximately 1 GHz working frequency [36]. Compared with the platforms working sequentially such as DSP, µC and PC, very high performance can be obtained from FPGA chips due to their some advantages such as parallel processing and system-specific design. Therefore, they can perform operations much faster than personal computers. Multiple copies of the design made inside FPGA chips can also be executed inside the chip. Moreover, with a standard computer and FPGA based custom computing machines, which is connected to this computer and contain one or more FPGA chips, designs can be carried out and high-performance platforms can be obtained. Because of these and similar advantages, in recent years, FPGA hardware has been widely used from motor control to industrial imaging, from Crypto communication to electronic warfare applications in space and defense industries, from digital cameras to Satellite Receivers in consumer electronics, from computerized tomography to ultrasound imaging in biomedical and from image processing to in-car information systems in automotive industry [37, 38]. Today, FPGA chips are manufactured by many companies such as Xilinx, Altera, Atmel, SiliconBlue, Microsemi and Lattice.

In general, FPGA equipment consists of three parts: input-output blocks (I-O blocks), interconnection network, and Configurable Logic Block (CLB). All of the Input-Output blocks (I-O blocks), connection network, and CLB structures can be configured. Input-output blocks can be used as input, output, or both input and output ports. Although their structure varies according to the type of chip, CLB units are generally composed of memory, logical blocks and multipliers. On the other hand, the interconnection networks are programmable

structures that provide the connection between the input-output ports and the CLB.

In FPGA chips, designs are carried out schematically and by using HDL (Hardware Description Language). VHDL and Verilog languages are the most preferred hardware description languages [39].

### *2.3 Numerical Algorithms*

In the literature, various algorithms were developed for numerical solutions of differential equations. Euler, Heun, fourth order Runge-Kutta (RK-4), fifth order Runge-Kutta Butcher and Dormant-Prince methods can be shown as examples of these algorithms. The Euler algorithm, one of these algorithms, is preferred because of its advantages such as being able to calculate numerical solution in a short time and easy modeling on digital processors. The Euler algorithm is given in the equation 2.

$$y_{\lambda+\Delta h} \approx y_{\lambda+1} = y_{\lambda} + f(y_{\lambda})\Delta h \quad (2)$$

In this equation, Δh refers to step range, $y_{\lambda}$ refers to initial value, and $y_{\lambda}+1$ refers to the values of the system to receive an iteration sonar. In the numeric algorithms used to be able to model continuous-time systems in real time on digital processors, in order to calculate the next $y_{\lambda}+1$ value of the system, $y_{\lambda}$, which is the previous value of it, is used.

## 3. FPGA-Based Van der Pol Oscillator

In this section, the Van der Pol oscillator is modelled to work on FPGA chips by using the Euler numerical algorithm and the 32-bit IEEE-754-1985 floating point number format [40]. The design was coded in VHDL, which is a hardware identification language. Units such as adders, dividers and subtractors in floating point number format, used in FPGA-based Van der Pol oscillator design, were created by using the IP Core generator presented with the Xilinx ISE Project Navigator program. In order to model the presented Van der Pol oscillator on FPGA chip, the discrete-time model of the system was created. In equation 3, using the Euler algorithm, a differentiated mathematical model of the Van der Pol system is presented.

$$\begin{aligned} w(k+1) &= w(k) + \Delta h\, w(k) \\ v(k+1) &= v(k) + \Delta h\left(-w(k) + \mu v(k) - \mu w(k)^2 v(k)\right) \end{aligned} \quad (3)$$

In the equation, intermediate values are calculated first by putting the w(K) and v(K) values in their place. Then, the calculated values are multiplied by Δh step range value. By summing the obtained values with the initial values of w(K) and v(K), the values of w(k+1) and v(k+1) are calculated, respectively. In this study, for the design of FPGA based Van der Pol oscillator, the Step range of Euler algorithm was taken as Δh=0.05 and μ=10.

The first-order block diagram for Modeling Van der Pol oscillator with Euler algorithm-based FPGA is given in Figure 2. One-bit Start and CLK signals at the entrance of the designed system are used to ensure the timing of all units and the synchronization between the units and the system to which the units are connected. In the design, while the initial values of the oscillator were embedded in the FPGA chip, the 32-bit initial conditions were embedded in the design to reduce resource utilization. However, when needed, the relevant signals can be taken out of the design by the designer. The FPGA-based Van der Pol oscillator unit has w_out and v_out 32-bit output signals in floating point standard and 1-bit Ready_wv signal used to indicate that these output signals are ready.

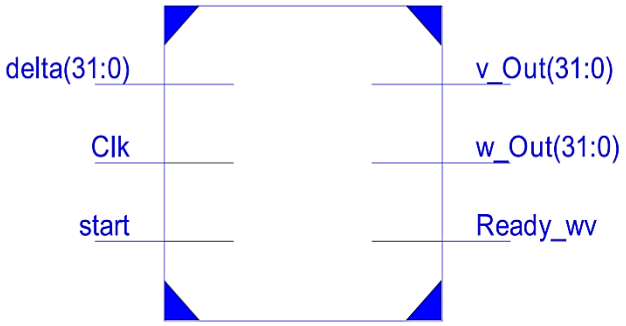


Figure 2. The first-order block diagram of FPGA-based chaotic Van der Pol oscillator

Figure 3 shows the second-order block diagram of the chaotic Van der Pol oscillator designed to operate in the FPGA chips. Designed system consists of 2 units; MUX and Euler units. The MUX unit serves as a selector for the starting conditions of the system and the signal produced by the oscillator. On the other side, the Euler unit is the unit that produces chaotic Van der Pol signals. When the '1' signal is applied to the start input of the design, the initial conditions required by the system are transferred to the Euler unit via the MUX. When the Euler unit generates its first value, the Ready_wv signal become '1', and at this time, the Van der Pol oscillator unit generates its first outputs as w_Out and v_Out. From this moment, the MUX unit sends the signals produced by the Euler unit to the system instead of the initial conditions.

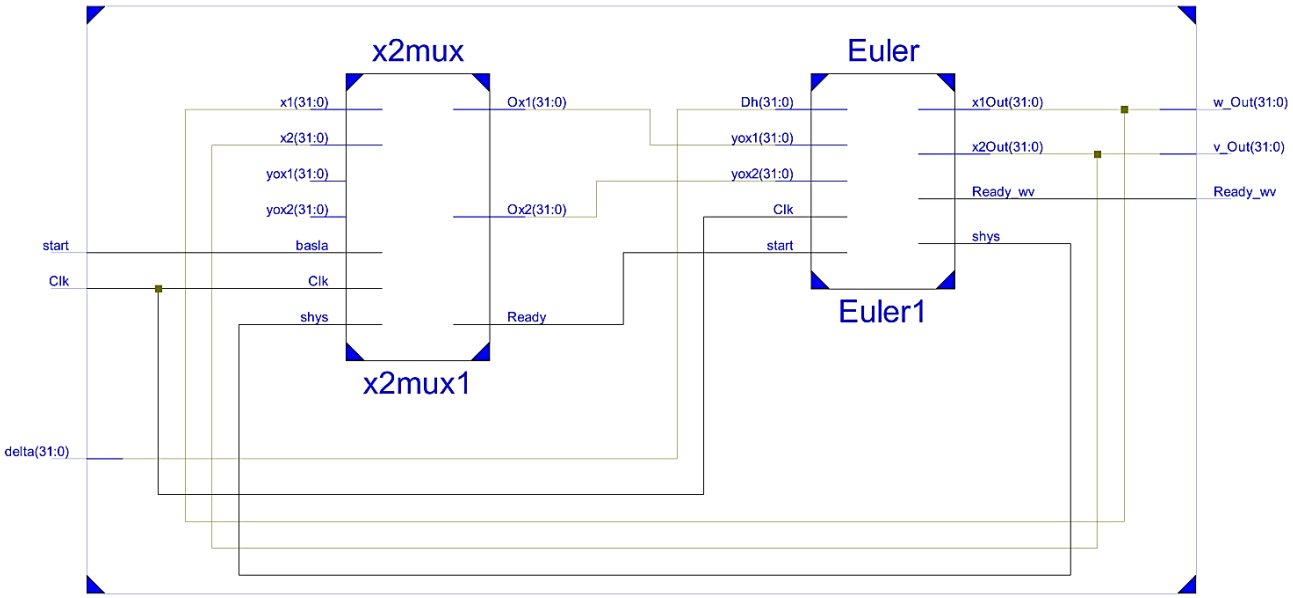


Figure 3: The second-order block diagram of FPGA-based chaotic Van der Pol oscillator

Figure 4 shows the third-order block diagram of the Euler-based chaotic Van der Pol oscillator unit. In the oscillator unit structure, there are 7 units including MUX, V, multiplication, addition and counter units. The V unit enables the calculation of w(k+1) and v(k+1) values in Van der Pol system equations with control signals coming from MUX unit. The signals obtained from the unit are summed in the addition unit with the start value signals (w(k) and v(k)), and the results are sent to the counter unit. Since the counter unit is designed as System pipeline, it is used to filter unwanted signals. The multiplication, addition, subtraction and other modules in the 32-bit floating point number format used in the Van der Pol oscillator, which was designed based on FPGA, were created by using the IP Core Generator developed by Xilinx Company. The Euler-based oscillator unit works as a pipeline, and the designed system produces the first result at the end of 128 clock cycles. In the next each 128 clock cycles, the system continues to produce a result. The designed chaotic Oscillator unit is tested by synthesized for the xc6vlx75t-3FF784 chip of the Virtex-6 Family produced by Xilinx Company. Figure 5 shows the simulation results of the Xilinx ISE Project Navigator program obtained from the realization of the Van der Pol chaotic generator on FPGA; this Van der Pol chaotic generator was designed by using Euler algorithm.

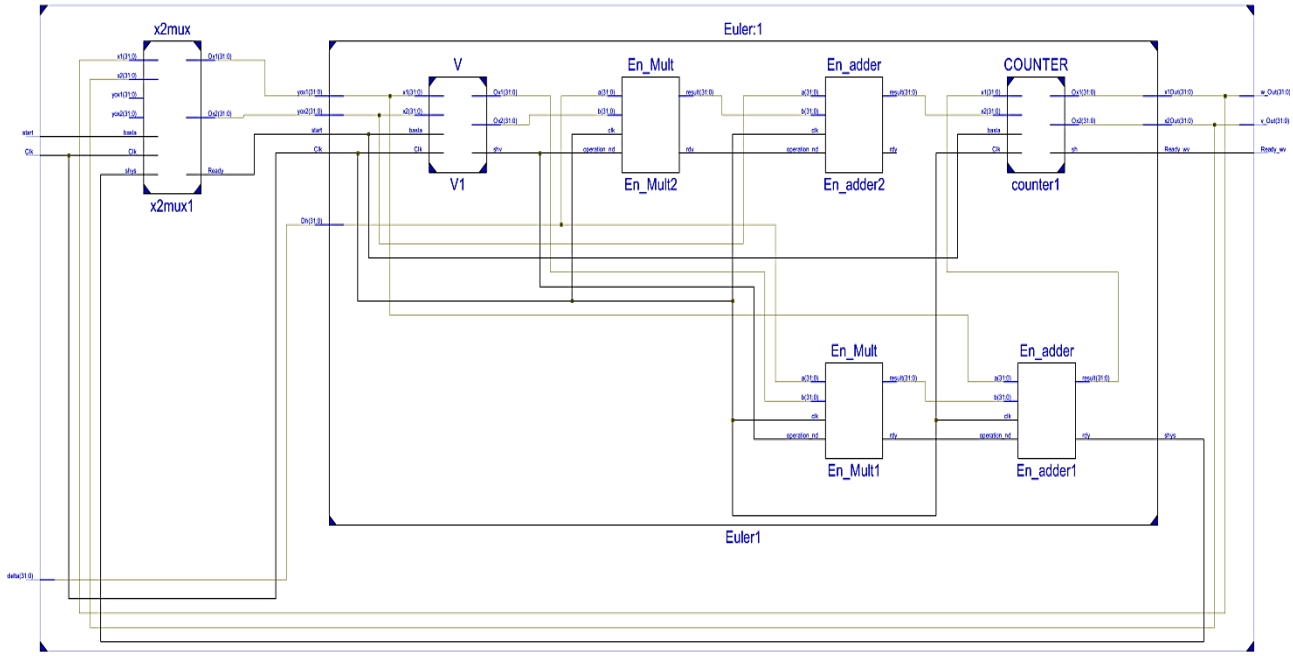


Figure 4: The third-order block diagram of FPGA-based chaotic Van der Pol oscillator

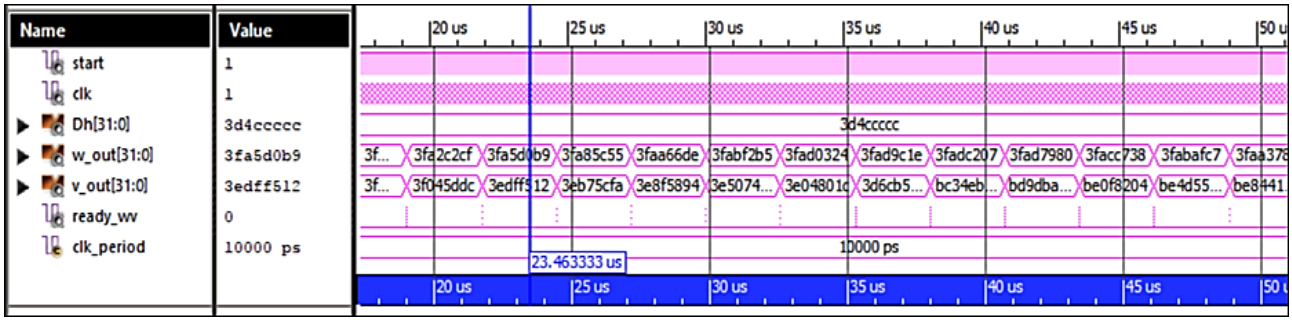


Figure 5: The simulation results of the Xilinx ISE Navigator of FPGA-Based Chaotic Van der Pol Oscillator Unit

The designed chaotic Van der Pol oscillator unit was realized using Euler algorithm on FPGA, and the FPGA chip statistics obtained from place and route process are given in Table 1. The maximum operating frequency of FPGA-based chaotic Van der Pol oscillator unit was obtained as 498.728 MHz. In other words, the minimum operating period of the designed unit is 2.005 ns.

Table 1. The usage statistics for Xilinx Virtex-6 XC6VLX75T-3FF784 chip of FPGA-based Van der Pol oscillator

| Logic Utilization | Used | Available | Utilization (%) |
|---|---|---|---|
| Number of Slice Registers | 4,702 | 93,120 | 5 |
| Number of Occupied slices | 1,326 | 11,640 | 11 |
| Number of Slice LUTs | 4,160 | 46,560 | 8 |
| Number of bonded IOBs | 99 | 360 | 27 |

## 4. Conclusions

In this study, for chaos-based engineering applications, Van der Pol oscillator was implemented by using the Euler algorithm on the FPGA. In the study, first the Van der Pol oscillator was numerically modelled and time-series were obtained. Then, using the numeric model, it was encoded on FPGA by using VHDL language and the Euler algorithm. In the design, 32-bit IEEE-754-1985 standard was used and it was synthesized by using the Xilinx ISE Project Navigator program. At the end of Place & Route process for Xilinx VIRTEX-6 chip family, the maximum operating frequency of FPGA-based Van der Pol oscillator unit was obtained as 498.728 MHz. The unit was tested by using Xilinx ISE Project Navigator program and test results were presented. In the future studies, random-number-generator design and synchronization applications will be able to be realized by using the FPGA-based Van der Pol oscillator presented in this study.

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