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Research Article

Performance analysis of SRF-PLL and DDSRF-PLL algorithms for grid interactive inverters

Fehmi Sevilmiş [a,*] ***and Hulusi Karaca*** [a]

[a] *Selçuk University, Faculty of Technology, Konya-42130, Turkey*

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ABSTRACT

In grid interactive power converter applications, phase locked loop (PLL) algorithms are very important to realize grid synchronization. The performance of PLL should not be affected by adverse conditions such as voltage unbalance, harmonics, frequency and phase changes. Otherwise, synchronization errors occur between the grid interactive inverter and the grid. In this paper, two different PLL algorithms are simulated by modeling under MATLAB/Simulink. The performances of the PLLs are comparatively presented under four different grid conditions such as balanced, unbalanced, harmonics and variable frequency. In this study, synchronous reference frame-PLL (SRF-PLL) and decoupled double synchronous reference frame-PLL (DDSRF-PLL) which are mostly used, state-of-arts and effective PLL algorithms are analyzed by modeling in grid synchronization applications. It has also been demonstrated the positive and negative aspects of the PLLs based on the obtained results.

1. Introduction

Phase lock loop (PLL) algorithm was first proposed by Appleton in 1923 [1]. After Appleton, Bellescize used the PLL algorithm to synchronize radio signals in 1932 [2]. Until the 1970s, the PLL could not find a wide range of applications due to the difficulty of its implementation. The PLL has begun to be largely used in modern communication systems by means of the rapid development of integrated-circuit (IC) technology in the 1970s. Later, it was used in different industrial fields such as speed control of electric motors and static power converters [3].

Nowadays, the PLL algorithm is also used as a new area to ensure synchronization in grid interactive inverters. In recent years, there has been an increase in use of the PLL in this field. The PLL must provide fast and precise synchronization between the inverter and the grid. Furthermore, it must have a good response to harmonics, imbalances, phase jump, frequency changes, and various disturbing effects in grid voltages. Therefore, PLL algorithm plays a major role for grid interactive inverters [3].

In Figure 1, block structure of the PLL is shown. This structure automatically synchronizes the phase of the output signal to the phase of the input signal as it is a feedback system [4]. The PLL structure consists of the phase detection (PD), the loop filter (LF) and the voltage controlled oscillator (VCO) blocks. The PD block determines the phase difference between input signal (V_i) and output signal. In addition, it produces a proper error signal [5], [6]. This error signal is transferred to the LF block. The LF demonstrates the low-pass-filter (LPF) characteristic to provide stability of the system. Moreover, it typically comprises of the first-order LPF or a proportional and integral (PI) controller. In other words, the LF block specifies the dynamics of the system [7], [8]. The signal at the output of the LF block generates the output signal in the same phase as the input signal by driving the VCO. Thereby, the output signal follows the input signal [9], [10].

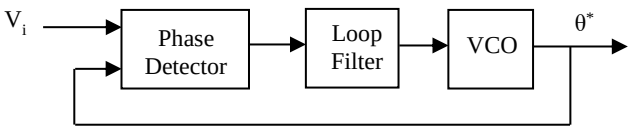

Figure 1. Block structure of the PLL

* Corresponding author. Tel.: +90-332-223-4396; Fax: +090-332-241-2179.
E-mail addresses: fehmisevilmis@selcuk.edu.tr *(F.Sevilmiş)*, hkaraca@selcuk.edu.tr *(H. Karaca)*
ORCID: *0000-0002-6059-9583 (F.Sevilmiş), 0000-0002-5561-489X (H. Karaca)*
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The aim of this paper is to compare the performances of two of the most preferred, state-of-arts and the most effective PLL algorithms under four different grid conditions such as balanced, unbalanced, harmonics and variable frequency. In this study, SRF-PLL and DDSRF-PLL algorithms have been modeled. The performances of the PLL methods have been compared based on the obtained results. The results have been presented in a comparative table and the advantages and disadvantages of these PLL algorithms have been pointed out. In this respect, according to the grid disturbances, PLL algorithm which should be preferred has been put forward.

This article is organized as follows: in the first section, the PLL algorithm is introduced and the purpose of the study is explained. In the second section, two different PLL algorithms and the block structures of each PLL algorithm are mentioned. In the third section, the PLLs with block structures are simulated in MATLAB/Simulink under different grid conditions such as balanced, unbalanced, harmonics and variable frequency, and their performances are compared. In the last section, the advantages and drawbacks of the PLLs are emphasized.

2. Phase Locked Loop Algorithms

2.1 Synchronous Reference Frame-PLL

The synchronous reference frame-phase locked loop (SRF-PLL) algorithm is used extensively in three-phase systems. In Figure 2, the block structure of SRF-PLL is shown.

The SRF-PLL operates as a feedback servo system to instantaneously detect the phase angle (θ) of the grid voltage. In this system, the three-phase grid voltages are firstly measured. Then, the measured three-phase grid voltages are transformed to the stationary frame variables (V_α, V_β) by Clarke rotation matrix given in Equation (1). After, the V_α and V_β voltages are converted to the rotating (synchronous) frame variables (V_d, V_q) by Park rotation matrix in Equation (2). The estimated phase angle (θ^*) of the grid voltage is fed back to operate the abc to dq block so that the Park rotation can be performed. That block also works like the PD block [11]-[13].

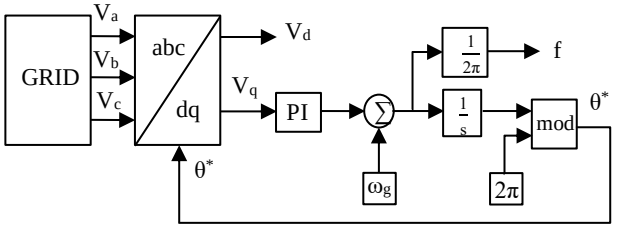

Figure 2. Block structure of the SRF-PLL

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} cos(\theta^*) & sin(\theta^*) \\ -sin(\theta^*) & cos(\theta^*) \end{bmatrix}\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (2)$$

In the SRF-PLL method, V_d and V_q voltages appear as DC components. In ideal grid conditions where the grid voltages are balanced and there are no harmonics or distortions, the estimated phase angle (θ^*) equals to the phase angle (θ) of the grid voltage. The estimated phase angle is the same as the phase angle of the voltage V_a of the grid. As can be seen from Equation (3) and Equation (4), V_q equals zero while V_d equals the peak value of the grid voltage. As can be understood from the equations, V_q contains information about the phase angle error of the grid. On the other hand, V_d gives the amplitude information of the grid voltage in steady-state. Besides, the SRF-PLL offers the estimated frequency (f) information [13]-[16].

$$V_q = V_m\, sin(\theta - \theta^*) \quad (3)$$

$$V_d = V_m\, cos(\theta - \theta^*) \quad (4)$$

In the loop filter design of the SRF-PLL, it is very important for the dynamic performance of the system that the estimated phase angle is fast locked to the phase of the grid and shows good filtering characteristics. However, in the SRF-PLL, these two conditions cannot be met at the same time. In ideal grid conditions, the high bandwidth of the filter ensures that the grid voltage and phase angle can be determined quickly and accurately [9]. If the grid voltage is disturbed by high-order harmonics, the band-width is reduced to ensure stable operation of the SRF-PLL, but in this case, synchronization time is increased. Moreover, V_d voltage cannot exactly determine. When imbalances in the grid voltage occur, reducing the band-width cannot stabilize the system. This problem can be solved by adding a simple low pass filter to the system. While the addition of low pass filter improves the stability of the system, it greatly reduces the dynamic response of the system [9], [17]-[18].

PI controller is usually used in the control algorithm of the SRF-PLL. The PI controller also works as a loop filter in the system, which controls V_q and detects the dynamics of the system. In order to determine the phase angle of the grid voltage fast and precisely, the PI parameters must be adjusted appropriately. In variable grid conditions, if the PI parameters are not adjusted properly, errors occur at the determined phase angle and the system works unstably [3], [15], [19].

While the SRF-PLL has a good response under ideal grid

conditions and variable frequency grid condition, it causes errors in determining the phase angle of the grid voltage under non-ideal grid conditions such as distorted and/or unbalanced [16], [19]. In non-ideal conditions, different filtering methods should be used [3], [4].

2.2 Decoupled Double Synchronous Reference Frame-PLL

Under unbalanced grid condition, positive sequence and negative sequence components of grid voltage occur. Since these components cannot be controlled independently in the SRF-PLL method, errors occur in synchronization between the inverter and the grid. The basis of the DDSRF-PLL algorithm is based on the conversion and independent control of the positive sequence and negative sequence components of the grid voltage. This algorithm highly removes the errors in determining the phase angle of the grid in the conventional SRF-PLL [20]. Furthermore, the DDSRF-PLL can be used in wind energy systems due to its very good response to grid frequency changes [21].

The DDSRF-PLL consists of the dq^{+1} frame rotating in positive direction (with angle θ) and the dq^{-1} frame rotating in negative direction (with angle -θ). The components of the dq^{+1} and dq^{-1} frame are given by Equation (5) and Equation (6), respectively [9], [20].

$$\begin{bmatrix} V_{d^{+1}} \\ V_{q^{+1}} \end{bmatrix} = \begin{bmatrix} V^*_{d^{+1}} \\ V^*_{q^{+1}} \end{bmatrix} + \begin{bmatrix} cos(2\theta^*) & sin(2\theta^*) \\ -sin(2\theta^*) & cos(2\theta^*) \end{bmatrix} \begin{bmatrix} \overline{V_{d^{-1}}} \\ \overline{V_{q^{-1}}} \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} V_{d^{-1}} \\ V_{q^{-1}} \end{bmatrix} = \begin{bmatrix} V^*_{d^{-1}} \\ V^*_{q^{-1}} \end{bmatrix} + \begin{bmatrix} cos(-2\theta^*) & sin(-2\theta^*) \\ -sin(-2\theta^*) & cos(-2\theta^*) \end{bmatrix} \begin{bmatrix} \overline{V_{d^{+1}}} \\ \overline{V_{q^{+1}}} \end{bmatrix} \quad (6)$$

As seen from the equations, coupled 2nd harmonic components (2ω) are added to positive and negative sequence components of V_d and V_q voltages. The positive and negative sequence components of the grid voltage are obtained in a decoupled manner by eliminating these coupled components.

Equation (5) and Equation (6) are rearranged to determine the decoupled components as in Equation (7) and Equation (8). In Figure 3 and Figure 4, block diagrams of these decoupled components are given.

$$\begin{bmatrix} V^*_{d^{+1}} \\ V^*_{q^{+1}} \end{bmatrix} = \begin{bmatrix} V_{d^{+1}} \\ V_{q^{+1}} \end{bmatrix} - \begin{bmatrix} cos(2\theta^*) & sin(2\theta^*) \\ -sin(2\theta^*) & cos(2\theta^*) \end{bmatrix} \begin{bmatrix} \overline{V_{d^{-1}}} \\ \overline{V_{q^{-1}}} \end{bmatrix} \quad (7)$$

$$\begin{bmatrix} V^*_{d^{-1}} \\ V^*_{q^{-1}} \end{bmatrix} = \begin{bmatrix} V_{d^{-1}} \\ V_{q^{-1}} \end{bmatrix} - \begin{bmatrix} cos(-2\theta^*) & sin(-2\theta^*) \\ -sin(-2\theta^*) & cos(-2\theta^*) \end{bmatrix} \begin{bmatrix} \overline{V_{d^{+1}}} \\ \overline{V_{q^{+1}}} \end{bmatrix} \quad (8)$$

In Figure 5, the block structure of DDSRF-PLL is given. This block structure is the extended form of the classical SRF-PLL block structure.

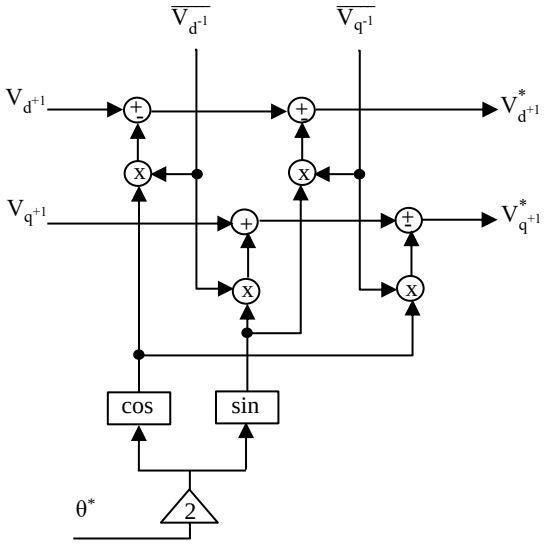

Figure 3. Block diagram of dq^{+1} decoupled components

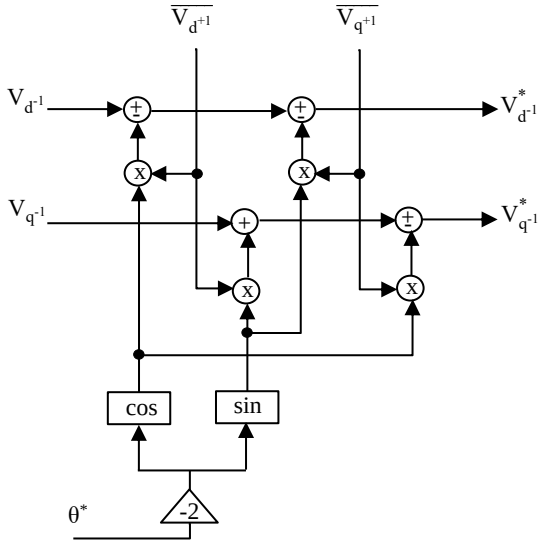

Figure 4. Block diagram of dq^{-1} decoupled components

With the DSRF-PLL algorithm, the actual amplitude value of the positive sequence voltage component is obtained exactly. The expression of the first order low-pass filter (LPF) shown in Figure 5 is given by Equation (9).

$$LPF(s) = \frac{\omega_f}{s + \omega_f} \quad (9)$$

The mathematical expression of the Park transform used for the positive sequence components ($\alpha\beta/dq^{+1}$) in Figure 5 is as in Equation (2). The mathematical expression of the Park transformation block used for the negative sequence components ($\alpha\beta/dq^{-1}$) is given by Equation (10).

$$\begin{bmatrix} V_{d^{-1}} \\ V_{q^{-1}} \end{bmatrix} = \begin{bmatrix} cos(\theta^*) & -sin(\theta^*) \\ sin(\theta^*) & cos(\theta^*) \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (10)$$

Since the DDSRF-PLL is one of the state-of-the-art PLL methods, many studies have been done to enhance the DDSF-PLL [22]-[25].

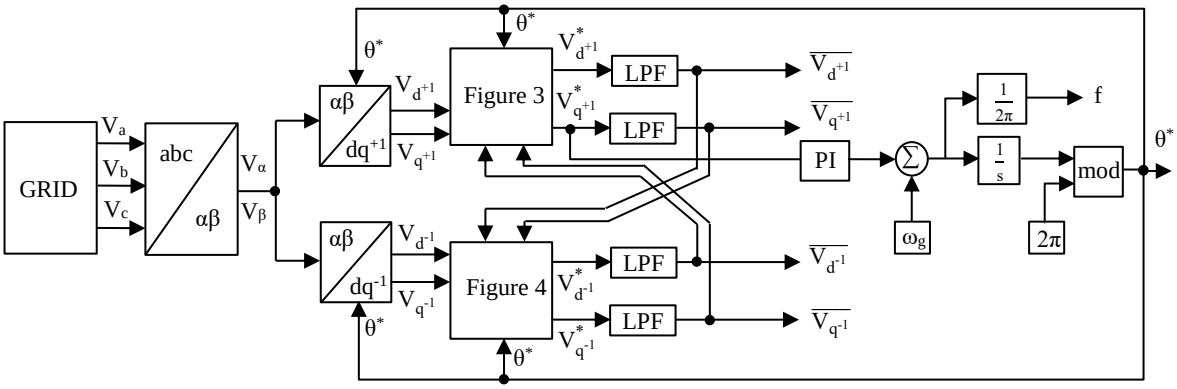

Figure 5. Block structure of the DDSRF-PLL

3. Simulation Results

In this section, the performances of phase locked loop algorithms are tested under different grid conditions. These are balanced, unbalanced, harmonics and variable frequency grid conditions. Simulations of PLL algorithms were performed in the MATLAB/Simulink environment. In the simulated PLL algorithms, the settling time was selected as 40 ms. In each PLL algorithm, PI coefficients were calculated by taking the damping ratio of the PLL loop filter as $\xi = 0.707$ and natural frequency $\omega_n = 162.63$ rad/s. Taking these parameters into consideration, $K_P = 0.74$ and $K_I = 85.05$ were obtained.

3.1 Unbalanced Grid Condition

In the first test, the PLL algorithms have been tested under unbalanced grid condition. As shown in Figure 6, the three-phase grid voltages are set to 311 V peak value and 50 Hz grid frequency under balanced grid condition until 0.1 s. Without frequency changes, harmonics and other disturbing effects are ignored. In simulation, the unbalanced grid phase voltages were injected to the system after 0.1 s. 373 V peak value for A-phase and 285 V peak value for B-phase and C-phase are used as unbalanced grid voltages.

Figure 7 and Figure 8 show the response of the SRF-PLL and DDSRF-PLL at unbalanced phase voltages, respectively. As seen in the figures, the SRF-PLL responds faster than the DDSRF-PLL under balanced grid condition (up to 0.1 s) due to its simple construction and low process requirements. However, the SRF-PLL causes a fault in determining the grid phase angle under unbalanced grid phase voltages. In this case, maximum phase error of SRF-PLL is 0.081 rad.

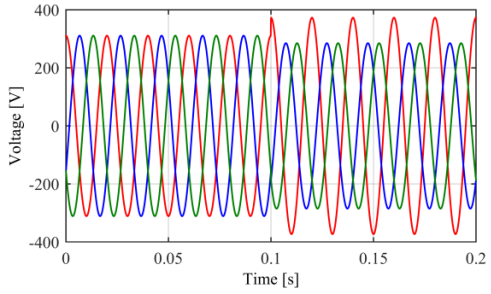

Figure 6. Three-phase unbalanced grid voltages

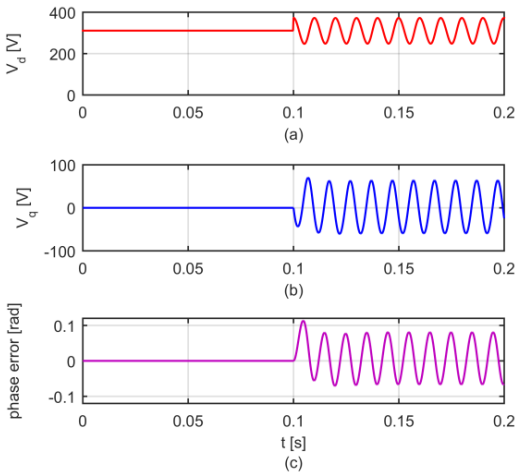

Figure 7. Response of the SRF-PLL under unbalanced grid condition (a) Change of V_d (b) Change of V_q (c) Phase error

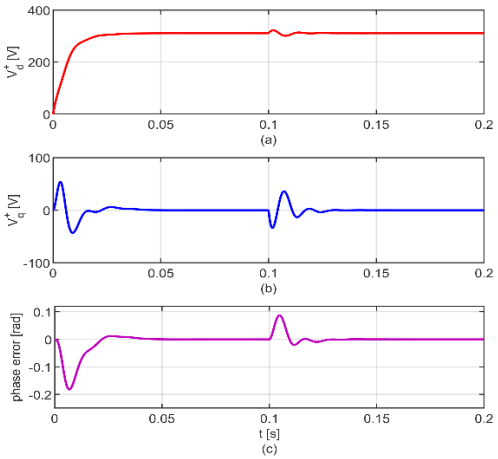

Figure 8. Response of the DDSRF-PLL under unbalanced grid condition (a) Change of V_d (b) Change of V_q (c) Phase error

In addition, since the positive sequence and negative sequence components of the grid phase voltage cannot be obtained independently, the effect of the second order harmonic component in the V_d and V_q voltages is clearly visible. In the DDSRF-PLL, as the positive sequence and negative sequence components of the grid phase voltage are obtained independently, the effects of the second order harmonic component in the V_d and V_q voltages disappear. Moreover, there is no phase error in steady state under unbalanced grid condition.

3.2 Grid Condition with Harmonics

In the second test, the responses of the PLL algorithms have been investigated by adding the fifth and seventh harmonic components to the grid voltages. The amplitudes of the added 5th and 7th harmonic components correspond to 10% (31 V) and 5% (15.5 V) of the grid voltage, respectively. The grid voltages are balanced and there is no change in the grid frequency. As shown in Figure 9, harmonics are added to the grid voltages after 0.1 s. Figure 10 and Figure 11 compare the performances of SRF-PLL and DDSRF-PLL algorithms, respectively.

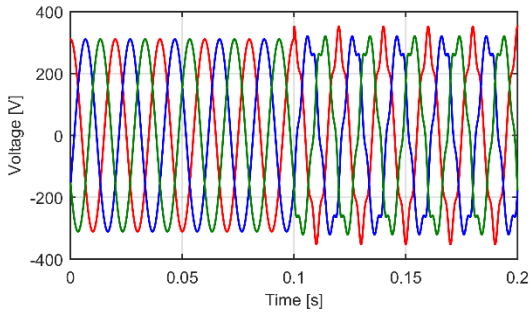

Figure 9. Three-phase harmonics grid voltages

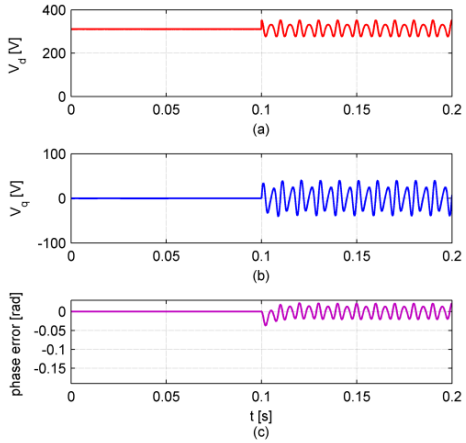

Figure 10. Response of SRF-PLL under grid condition with harmonics (a) Change of V_d (b) Change of V_q (c) Phase error

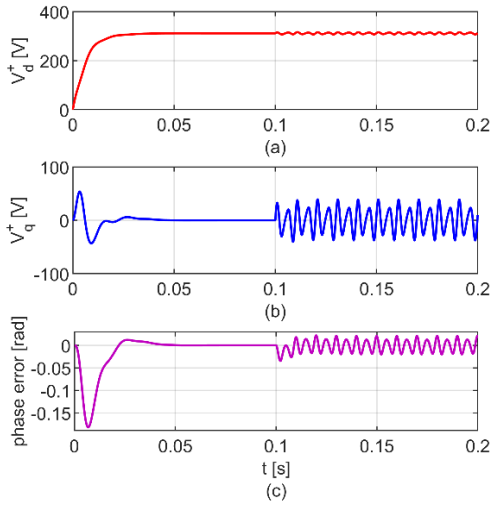

Figure 11. Response of DDSRF-PLL under grid condition with harmonics (a) Change of V_d (b) Change of V_q (c) Phase error

As can be seen from the figures, the response of the SRF-PLL and DDSRF-PLL to the harmonics is not good and causes a fault in determining the phase angle (maximum phase error = 0.021 rad). In both PLLs, when the bandwidth of the filter is reduced, their performances improve; however, the synchronization times are longer. While the estimated V_d voltage in SRF-PLL fluctuates between 273 V and 357 V, it fluctuates between 306 V and 316 V in DDSRF-PLL. Although the phase errors are the same, DDSRF-PLL estimates the V_d voltage more accurately than the SRF-PLL.

3.2 Variable Frequency Grid Condition

In the last test, the responses of the PLL algorithms have been tested under variable frequency grid condition. As can be seen in Figure 12, the frequency of the grid voltages has been increased from 50 Hz to 55 Hz at the time of 0.1 s, the grid frequency has been decreased from 55 Hz to 45 Hz at the time of 0.2 s and the grid frequency has been increased from 45 Hz to 50 Hz at the time of 0.3 s. It is assumed that the grid voltages are balanced and there are no harmonics or other disturbing effects. Figure 13 and Figure 14 show the responses of the SRF-PLL and DDSRF-PLL algorithms, respectively.

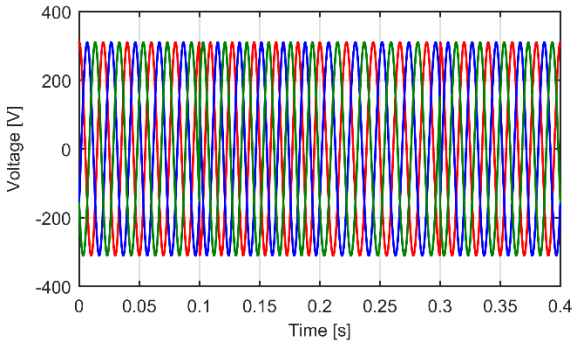

Figure 12. Three-phase variable frequency grid voltages

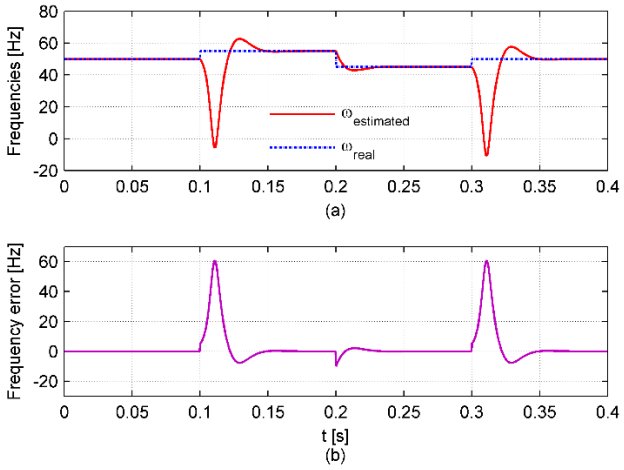

Figure 13. Response of the SRF-PLL under variable frequency grid condition (a) Real and estimated grid frequency (b) Frequency error

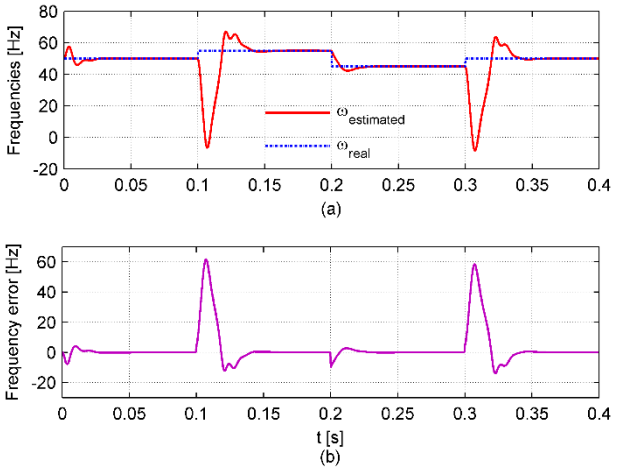

Figure 14. Response of the DDSRF-PLL under variable frequency grid condition (a) Real and estimated grid frequency (b) Frequency error

As can be understood from the figures, the performances of SRF-PLL and DDSRF-PLL against frequency changes are almost the same. In the case of the variable frequency grid, the maximum overshoot value of the SRF-PLL is 8 Hz while it is 13 Hz in the DDSRF-PLL. On the other hand, the SRF-PLL and DDSRF-PLL algorithms have an average settling time of 65 ms. There is no steady-state error in each PLL algorithms. Thus, the phase angle of the grid is determined without error in both PLL algorithms.

Finally, the PLL algorithm which should be preferred according to different grid conditions is presented in Table 1. If the grid interactive inverter is used only for a balanced and/or variable frequency grid condition, the SRF-PLL is more suitable to prefer. If the grid interactive inverter is used only for an unbalanced and/or harmonics grid condition, the DDSRF-PLL is more suitable.

Table 1. PLL preference for different grid conditions

Grid condition	**PLL preference**
Balanced	SRF
Unbalanced	DDSRF
Harmonics	DDSRF
Variable frequency	SRF
Unbalanced + Harmonics	DDSRF
Unbalanced + Variable frequency	DDSRF
Harmonics + Variable frequency	DDSRF
Unbalanced + Harmonics + Variable frequency	DDSRF

4. Conclusions

In this study, two different phase locked loop algorithms for grid synchronization are presented comparatively. The SRF-PLL and DDSRF-PLL algorithms are simulated in MATLAB/Simulink software. Based on the results obtained from these simulations, the performances of PLLs are compared under different conditions.

As a result of the findings, the SRF-PLL stands out with its simplicity, easy applicability and frequency response. However, under non-ideal grid conditions such as unbalanced and/or harmonic grid, the stability of the system becomes worse. On the other hand, since the DDSRF-PLL algorithm can accurately obtain positive and negative sequence components and the filtering capacity is high, the response and accuracy in such adverse conditions are at a desired level. The results of comparative simulations clearly demonstrate the importance of the PLL algorithm which should be preferred according to the grid distortions.

Nomenclature

LPF	: Low-pass filter
PI	: Proportional + Integral
V_a	: A-phase voltage of grid
V_b	: B-phase voltage of grid
V_c	: C-phase voltage of grid
V_α	: Stationary frame variable
V_β	: Stationary frame variable
V_d	: Synchronous frame variable
V_i	: Voltage of input signal
V_q	: Synchronous frame variable
θ	: Phase angle of grid voltage
θ^*	: Obtained phase angle
ω_g	: Angular frequency of grid voltage

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