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EFFECT OF SURFACE STATES ON ELECTRICAL CHARACTERISTIC OF METAL-INSULATOR-SEMICONDUCTOR (MIS) DIODES

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ABSTRACT

The current-voltage (*I-V*) characteristics of Metal-Semiconductor Schottky barrier diodes which is studied. Distribution of interface states in equilibrium with semiconductor were determined at two (low and high) temperatures. The interface states were responsible for non-ideal behavior of the forward *I-V* characteristic of diodes. Both diodes (*n* and *p* type Si) showed non-ideal behav-ior with an ideality factor (n) 1.6 and 1.85 respectively at room temperature. The higher values of ideality factor (n) were attributed to an order of magnitude higher density of interface states in the both p and n type Schottky diodes. The effect of an interfacial insulator layer between the metal and semiconductor are also studied. The high density of interface states also caused a reduction in the barrier height of the Schottky diode. It is shown that by using developed Norde function at each temperature, barrier height Φ_b, series resistance R_s and ideality factor n can be determined even in the case $1<n<\gamma$. The ideality factor n and series resistance R_s obtained from Norde function strongly depend on temperature, and decrease with increasing temperature. In addition, the potential barrier height increases with increasing temperature. The mean density of interface states N_{ss} decreases with increasing temperature. Particularly at low temperature the I-V characteristics are controlled by interface states density.

Key Words: Interface states, temperature dependent, oxide layer, I-V characteristics

ARAYÜZEY DURUMLARININ MIS TİPİ DİYOTLARDA ELEKTRİKSEL KARAKTERİSTİKLERE ETKİSİ

ÖZET

Metal-yarıiletken Schottky engel diyotlarında yarıiletkenle dengede olduğu kabul edilen arayüzey durumların dağılımı düşük ve yüksek sıcaklıkta akım-voltaj (I-V) karakteristiklerinden hesaplandı. Schottky diyotların doğru besleme I-V karakteristiklerinde ideal olmayan davranışı arayüzey durumlarından dolayıdır. Oda sıcaklığında idealite faktörü sırasıyla 1,6 ve 1,85 olan n ve p tipi Schottky diyotları ideal olmayan bir davranış gösterdi. İdealite faktörünün hem n hem de p tipi Schottky diyotunda yüksek çıkması arayüzey durumlarının yüksek olmasına atfedildi. Metal ile yarıiletken arasındaki yalıtkan arayüzey tabakasının etkisi incelendi. Yüksek yoğunluklu arayüzey durumları aynı zamanda Schottky

diyotunda engel yüksekliği düşmesine neden olur. Norde fonksiyonu kullanılarak Schottky diyotunda idealite faktörünün $1<n<\gamma$ olması durumunda bile her sıcaklıkta engel yüksekliği Φ_b, seri direnç R_s ve idealite faktörünün hesaplanabileceği gösterildi. Norde fonksiyonundan hesaplanan idealite faktörü(n) ve seri direncin(R_s) kuvvetlice sıcaklığa bağlıdır ve artan sıcaklıkla azalmaktadır. Buna ilaveten potansiyel engel yüksekliği (saf T.E. teorisine göre hesaplanan) ise artan sıcaklıkla azalmaktadır. Arayüzey durumlarının yoğunluğu artan sıcaklıkla azalmaktadır. Özellikle düşük sıcaklıklarda I-V karakte-ristiği arayüzey durumları tarafından kontrol edilmektedir.

Anahtar Kelimeler: Arayüzey durumları; sıcaklığa bağlılık; oksit tabaka; I-V karakteristikleri

1. INTRODUCTION

The existence of an interfacial insulator layer between the metal and semiconductor (native or deposited) transform the metal-semiconductor (MS) structure into a metal-insulator-semiconductor (MIS) diode with capacitance-voltage (*C-V*) characteristics the slope and inter-cept voltage of which will consequently deviate from those expected for an ideal Schottky di-ode. The interfacial insulator layer, interface states and series resistance, have an especially strong influence on the forward bias *I-V* and *C-V* characteristics of MIS structures. Recently the *C-V* and *I-V* characteristics of Schottky diodes have been the subject of intensive work (1-11), in particular, the effect of the series resistance on the capacitance of Schottky diode has been investigated (3,6,11). However this method is limited to a Schottky barrier with an ultra thin interfacial layer and moderate doping concentration. Discussions relating to presence of the thin interfacial layer film (3) usually begin with the assumption that the interface states are in equi-librium with the metal. Measurements on silicon Schottky diodes indicate that this is not the case. The density of interface states is dependent upon the thickness of the interfacial insulator layer film (8). For the states that are located at the silicon-oxide interface the communication with the metal decreases with increasing layer film thickness.

In this work, the energy density distribution of the interface states was obtained from the forward bias (I-V) characteristics at two different temperatures (low and high temperature). In addition, it was shown that by using Bohlin et al. (13) approach at two different temperatures series resistance, the value of ideality factor (n) and barrier height can be determined even in the case $1<n<\gamma$. We also report on a new formalism to analyze the current-voltage characteristics in an MIS type diode. This formalism considers the effect of voltage and interfacial layer thickness dependent barrier height, ideality factor and distribution of interface states.

2. THEORETICAL BACKGROUND

The energy - band diagram of a metal-semiconductor-pSi Schottky diode with an inter-facial insulator layer and a series resistance under forward bias condition is shown in Fig.1 In the figure, $q\Phi_m$ represents the work function of the metal, Δ the potential drop across the oxide layer, δ the thickness of the SiO_2 layer, Φ_0 the neutral level, Ψ_s the surface potential, the posi-tive signs represent fixed charge in the oxide layer, $q\chi$ the electron affinity of the semiconduc-tor, and Φ_0 the energy level at the surface. IR_s represents the voltage drop across the series resis-tance, where I is the forward current across the device. For a Schottky diode with a thin interfa-cial oxide layer between metal and semiconductor, the thermionic emission (TE) theory predicts that the relation between the applied forward voltage V and current I, is given by (8).

$$I = I_0 \exp(qV/nkT)\left[1-\exp(-qV/kT)\right] \quad [1]$$

If a MIS diode has a uniform oxide layer, then the current expression can be written as (5).

$$I = A^{*}AT^{2}\exp(-q\phi_{b}/kT)\exp(-\chi^{1/2}\delta)\exp[qV/(1+q^{2}\delta\ D_{it}/\varepsilon_{i})kT] \quad [2]$$

Where $V(=V_a - IR_s)$ is the voltage drop across the rectifying barrier and is defined by V_a is the applied voltage, R_s is the diode series resistance, n the ideality factor, the term $\exp(-\chi^{1/2}\delta)$ is commonly known as tunneling factor and can be obtained from Eq. (2), δ is the interfacial oxide layer thickness. The saturation current I_0 described by (6):

$$I_0 = AA^{*}T^{2}\exp(-q\Phi_b/kT) \quad [3]$$

Where A is the MIS diode area, A^* is the effective Richardson constant, T is the temperature in Kelvin, k is the Boltzman constant, and Φ_b is the barrier height. It is customary to make ln (I) vs V plots at various temperatures and extract from the straight-line portion the reverse satura-tion current (I_0) by extrapolation to zero-bias and the ideality factor from the slope itself. Also, R_s data are found from the experimental I-V data using the Norde function.

The Norde function can be modified for the case of $1<n<\gamma$

$$F(V,\gamma)=V/\gamma-(kT/q)Ln(I/AA^{*}T^{2}) \quad [4]$$

Where γ is an arbitrary constant greater than the ideality factor n. Once I_0 is known, the barrier height Φ_b can easily be determined from Eq.(3) at any temperature for a given diode area A and Richard-son constant A^*(32 A cm^{-2} K^{-2} for p-type Si and 112 A cm^{-2} K^{2} for n-type Si) (8).

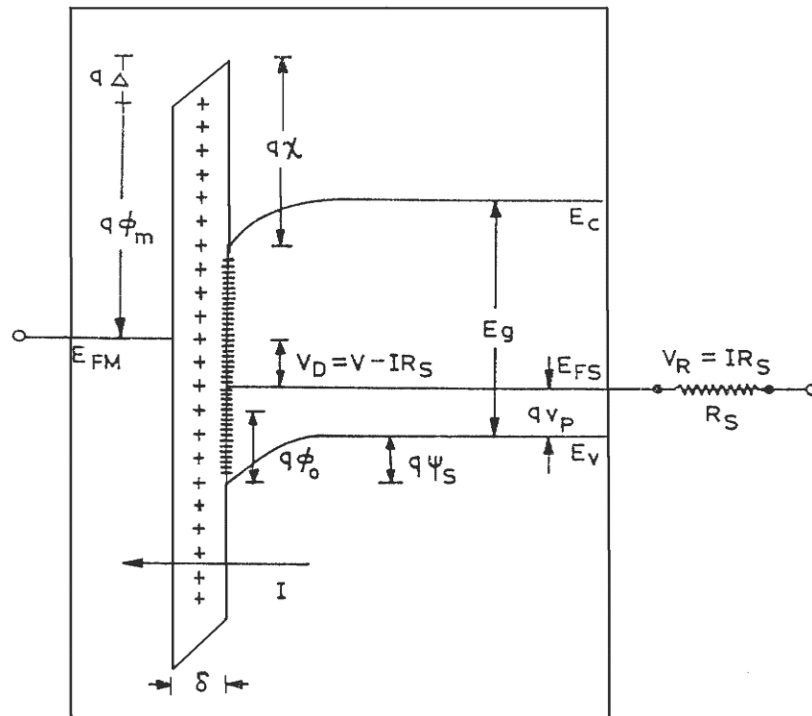

Fig.1. Energy band diagram of MIS diode with an SiO_2 interfacial oxide layer.

The voltage dependence barrier height is contained in the ideality factor (n) through the relation [The effective barrier height Φ_e is contained in the ideality factor n through the relation].

$$\frac{\delta\phi_e}{\delta V} = \Gamma = 1 - \frac{1}{n} \qquad [5]$$

Where Γ is the voltage coefficient of the effective barrier height Φ_e. which is given by,

$$\Phi_e = \Phi_b + \left(1 - \frac{1}{n}\right)V \qquad [6]$$

The ideality factor (n) is related to the oxide thickness and interface states density by the relation (9). For an MIS diode, the ideality factor n becomes greater than unity as proposed by Card and Rhoderick (5).

$$n = 1 + \left[\frac{\varepsilon_s}{W} + qN_{ss}\right]\frac{\delta}{\varepsilon_i} \qquad [7]$$

Where ε_s and ε_i are the permitivity of the semiconductor and the interfacial layer respectively, W is the space charge width, and N_{ss} is density of the interface states in equilibrium with the semiconductor. In a p-type semiconductor, the energy of the interface states E_{ss} with respect to the top of the valence band at the surface of the semiconductor is given by

$$E_{ss} - E_v = q(\Phi_e - V) \qquad [8]$$

Pandovani and Stratton (14) have pointed out that at moderate temperatures and doping levels, thermionic-field emission (TFE) is responsible for current transport, and forward I-V characteristics, except for very low forward biases. In this study, we have attempted to analyze the current-voltage (I-V) characteristics of a metal-insulator-semiconductor (Al/SiO_2/p-Si and Au/SiO_2/n-Si) (MIS) device, considering a bias and temperature dependant density distribution of the interface states.

3. EXPERIMENTAL

Several diodes of the Al/p-Si and Au/n-Si structures were fabricated on half of the 2 inch diameter float zone <100> p-type (boron doped for p-type Si and phosphorous doped for n-type Si) single crystal silicon layer (with thickness 500 μm, $\approx 1\ \Omega$ cm resistively). Samples were ul-trasonically degreased by dipping into isopropyl alcohol, and washed with de-ionised water, then chemically etched with a CP4 (HF: CH_3COOH: HNO_3: 1:1:2) solution for 3 min. In order to remove the native oxide layer before making contacts, the samples were dipped into a HF: H_2O (1:15) solution for 3 min. High purity (99.999 %) aluminium with a thickness of 2000 Å was thermally evaporated from the tungsten filament onto the whole back side of in half layer at a pressure of $2x10^{-6}$ Torr in a vacuum system. 2000 Å thick aluminium dots of 2 mm diameter were evaporated onto the front contact. The I-V characteristic of both p-type and n-type Si MIS diodes with, a native oxide layer at two different temperatures (low and high) were measured. This measurements were performed by the use of a Keithley 220 programmable constant current source and a Keithley 614 electrometer, and the temperature was controlled by using a VPF-100 cryostat system.

4. RESULTS and DISCUSSIONS

Fig.2. (a) and (b) shows the dark forward bias LnI-V characteristic of the Al/SiO_2 /p-Si and Au/ SiO_2/n-Si MIS diodes with 30 Å oxide layer thickness at two different temperatures. The Line-V curves consist of two linear regions at low temperature for the two types diode, but at high temperature, these curves have only one linear region. At low temperatures, it is observed that the LnI-V characteristics show a strong tendency towards quantum-mechanical tunneling (14). The ideality factor n was obtained as a function of the applied voltage at two different temperatures (low and high) for Al/p-Si and Au/n-Si diodes. The behavior of the ideality factor n is similar in both Al/p-Si

and Au/n-Si diodes and increases with increasing voltage. The ideality factor n decreases with increasing temperature. For the fabricated diodes, the values of the ideality factor are appreciably higher then expected. This is due to the high density of interface states which are localised in the Si energy bandgap.

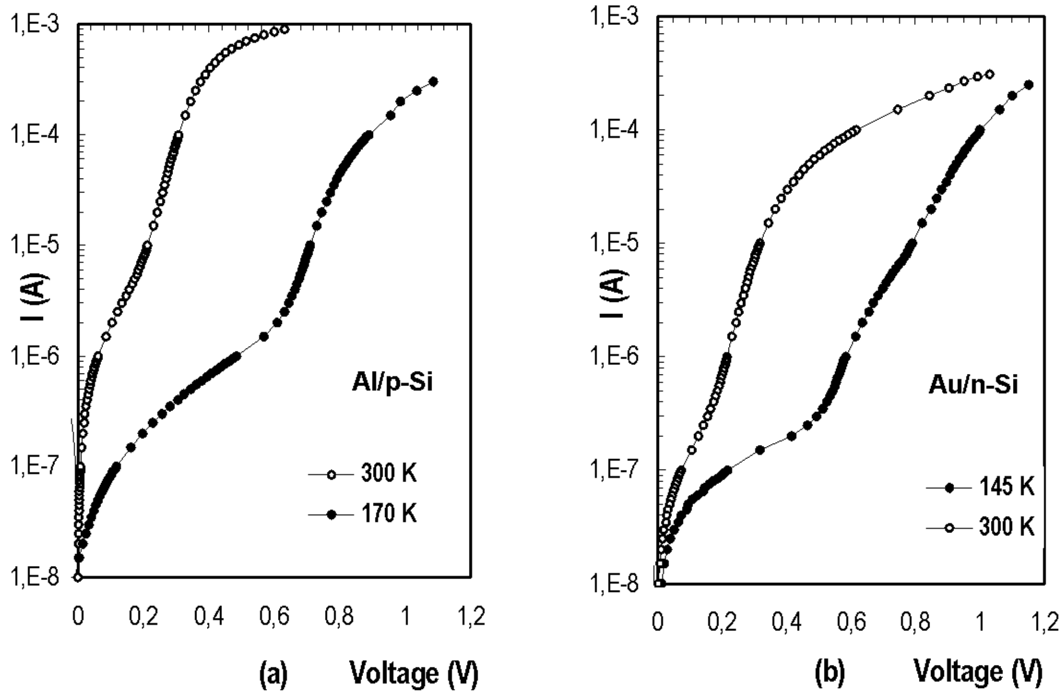

Fig.2. Forward I-V characteristics of Al/SiO_2/p-Si and Al/SiO_2/n-Si MIS structures respectively for two different temperature.

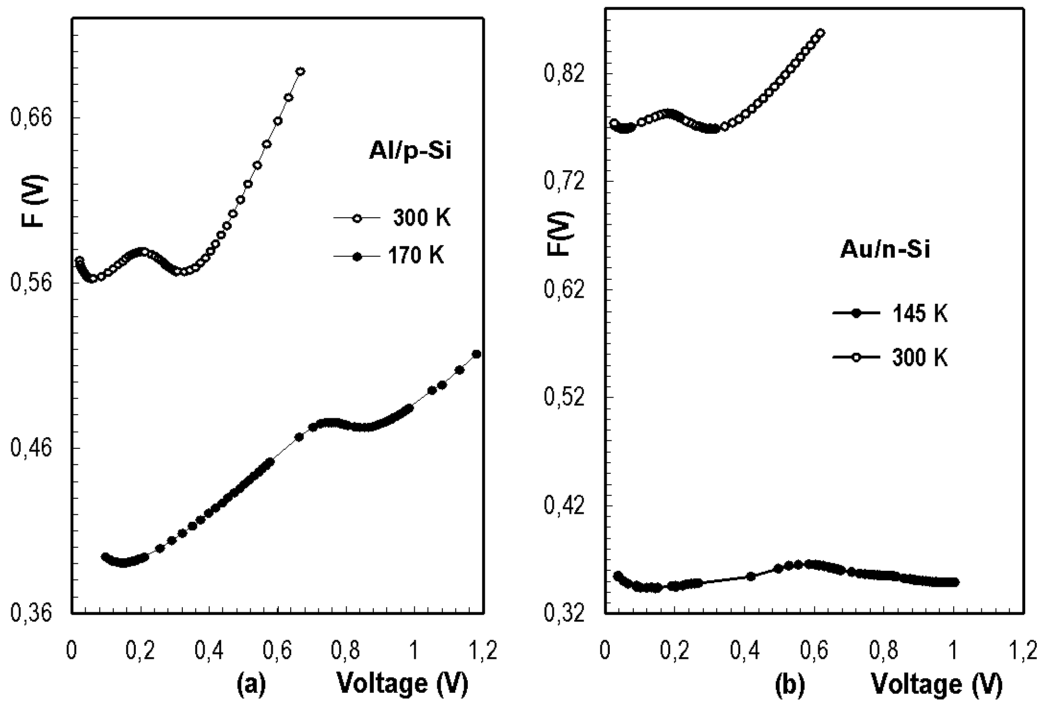

Fig.3. F(V)-V plots of Al/SiO_2/p-Si and Al/SiO_2/n-Si MIS structures respectively for two different temperature.

In Fig.3. (a) and (b) shown F(V) vs V obtained from I-V data using equation [4] at two different temperatures. F(V) plots have a minimum point, and we can calculate the series resistance at any temperature from this minimum [R_s = kT(γ -n)/qI_0]. At low temperature, the calculated series resistance R_s, and ideality factor n values are higher than at high temperatures one for both type of diodes. In addition, the potential barrier height Φ_b value increases as temperatures one for increase. Such temperature dependence is in obvious disagreement with the reported negative coefficient of the barrier height. This contradiction is possibly due to Eq. [3] which is not representing the reverse saturation current Io in our MIS samples, implying that the carrier transport is not the thermionic mechanism. Similar results have been reported in the literature (10, 13, 15, 16).

Using two I-V curves at two different temperatures, the main parameters of a MIS diode, that is, the Schottky barrier height Φ_b , series resistance R_s and ideality factor n can be calculated. At two temperatures, values of various electrical parameters determined from I-V characteristics are given in Table 1.(a) and 1.(b) for n-type and p- type MIS diodes respectively.

Table 1. (a) At two different temperatures values of various parameters of Au/n-Si MIS diode.

T [K]	n	V_{min} [V]	I_{min} [mA]	F(V_{min}) [V]	R_s [Ω]	Φ_b(F-V) [eV]
145	3.60	0.80	0.25	0.417	55.00	0.452
300	1.60	0.22	1.5	0.720	24.95	0.986

Table 1. (b) At two different temperature values of various parameters of Al/p-Si MIS diode.

T [K]	n	V_{min} [V]	I_{min} [mA]	F(V_{min}) [V]	R_s [Ω]	Φ_b(F-V) [eV]
170	3.00	0.85	0.30	0.314	48.88	0.475
300	1.85	0.25	1.00	0.68	29.75	0.919

Substituting in Eq. [7] for each temperature, the values of n related to bias V and the variation of the depletion width WD calculated from the C-V characteristics and taking $\varepsilon_i = 3.8 \times \varepsilon_0$ and $\varepsilon_s = 11.8 \times \varepsilon_0$ (9), we can evaluate the states density Nss variation related to bias V.

In Fig. 4. (b) and (d), we have plotted N_{ss} vs (E_c-E_{ss}) for n-type and N_{ss} vs (E_{ss}-E_v) for p-type MIS diodes using Eq.[8]. We observe then that the density of interface states Nss decreases with increasing temperature for both p-type and n-type MIS diodes. This improvement is due to rerestructuring and reordering of the semiconductor-metal interface as the temperature is increased.

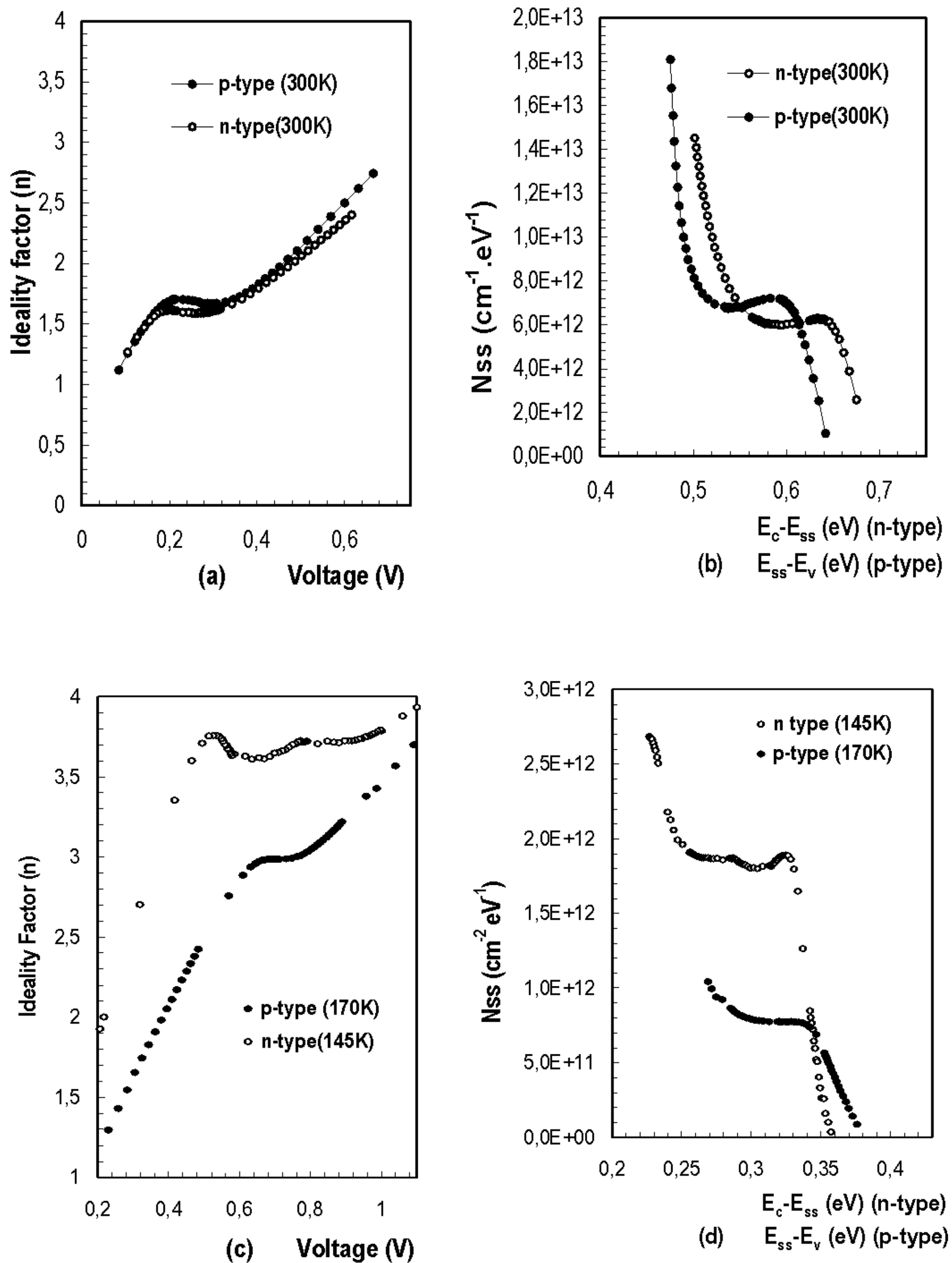

Fig.4. (a) and (c) n vs V for two type MIS diode (b) and (d) density of interface states as a function of Ec-Ess(eV) for n-type or Ess-Ev (eV) for p-type

5. CONCLUSION

Both p-type and n-type Schottky diode I-V characteristics exhibited unusually linear behaviours particularly at low temperature. In both the Al/p-Si and Au/n-Si diodes, the barrier height Φ_b increased with the forward bias, which suggested that the interface states in those diodes were in equilibrium with the semiconductor. The ideality factor n and density of interface states decreases

with increasing temperatures.The Schottky barrier height Φ_b increases with increasing temperature and this increase conflicts with the literature. This result indicates that these diodes deviate from the pure thermionic-emission theory due to contribution of another current transport mechanism(such as thermionic field emission or field emission), particularly at low temperature. The higher value of the ideality factor n was attributed to an order of magnitude higher density distribution of interface states. The I (V) curve is not ideal and the ideality factor is controlled by the interfacial states density. The interfacial states den-sity, non uniformly distributed in the semiconductor band gap, is reversibly proportional to tem-perature. The ideality factor n and series resistance Rs obtained forward bias I-V measurement strongly depends on temperature and decrease with increasing temperature.

We have obtained the profile density of interface states, in both halves of the energy gap on n- and p-Si wafers prepared under identical conditions using the I-V technique at two temperatures(low and high). The density of interface states non-uniformaly distributed in the semicunductor bandgap and increasing with, decreasing temperature. This improvement is the result of molecular restructuring and reordering at the metal-semicunductor interface [17]. The advantage of lowering the temperature is the ability to measure interface states not normally accessible at room temperature. Consequently, ideality factor n, the density of interface states Nss , and series resistance Rs are strongly dependent on temperature.

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