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Redesign of Development Board for Engineering Education

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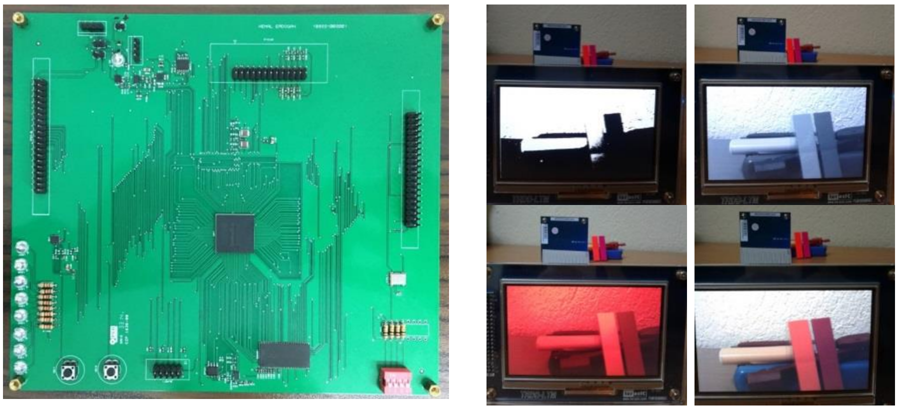
HIGHLIGHTS

- The produced board
- Real time operations on the input images

GRAPHICAL ABSTRACT



a) *b)*

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ABSTRACT

With the rapid developments in technology, devices used in engineering applications are being renewed continuously. But sometimes this renewing process costs higher prices. For this reason there could be some delays at this point and this may cause a decrease in the quality of education. In this study, it is tried to find a solution to the problem of outdated devices used in electronics engineering education. A multi-layered and complex FPGA (Field Programmable Gate Array) development board has been transformed into a more simple and updateable form which is consisting of two layers. By this way, the development card can be easily adapted to the different projects needed in electronic engineering education.

1. INTRODUCTION

Nowadays, electronic boards are used almost in every part of our life. One of the most important component of these systems is FPGA. FPGA development boards are produced for developing and training FPGA based applications. Several circuit components needed according to user demand and to program the FPGA could be present on these development boards.

FPGAs are used in a lot of fields like digital signal and image processing, medical imaging, military and automotive industry etc. FPGAs are capable of parallel processing and allowing to update the hardware by changing the software. Because of these advantages, they are frequently preferred in intensive processing power needing real time applications like image and video processing applications [1]. An important feature needed in electronics engineering education is that the board can be updated. Sometimes it is desired to make improvements on these types of boards according to the position used. Although FPGAs allow revisions on hardware without physical interventions, the input/output units are generally not allowed to modify because of the design of the producer and the complex structure of the printed PCB. This problem and the rapid technological improvements lead to make development boards functionless in a small time period for engineering education.

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On the other hand, small amount of power consume would make advantage for a system. These types of systems could be fed with a solar cell in environments without power line. Sometimes unneeded components for a project should be removed to decrease power consumption. To adapt the board to one of these situations, the hardware of the board would be needed to update. With this study, redesign of a development board which could be used for image or video processing applications in electronics engineering education and whose input / output components could be updated easily was realized. This non-commercial and academic purposed study is a redesign of a development board of Terasic Company [2, 3]. This six layered, small but complex PCB design was changed into a simpler, cheaper but bigger design which is having easily updatable input/output units. With this reinterpretation, the development board would be able to be used for different projects for engineering education.
Instead of needed components on FPGA development board, a camera and an LCD display are used in this study. In the application executed on the board, the image taken from camera is shown on LCD. This color image is modified as (black and white, grey level and red level) according to the logic input which is get from a dip switch.

2. RELATED WORKS

First FPGA production was realized by Ross Freeman and Bernard Vonderschmitt who are the establishers of Xilinx company with the model XC2064 in 1985 [4]. Studies in the literature show that FPGAs are used in real time image processing applications successfully.
D. Crookes et al. offered the redesignable hardware in FPGA form as an alternative method to obtain high performance for the digital signal processing applications under real time needs [5]. The reprogrammability of FPGA provides the software flexibility besides the performance advantage.
Peter Mc Curry et al. used FPGA for an image classifier to recognize images. They compared its performance according to DSP (Digital Signal Processor) based systems and declared that FPGA based system showed higher performance [6].
Uzun et al. explained the need of high computational power in addition to the training ability of algoirthms for FFT (Fast Fourier Transform) based marker and image processing applications. They told FPGA based hardware devices have economical prices and higher performances. However, FPGAs are needed to program in low level and their architecture should be known in detail. They concluded that FPGA is a suitable solution for implementing the 2 dimensional FFT based image filtering application on it [7].
Huitzil and Estrada mentioned that the pattern processing requires more computational power and data flow capability than conventional processors provide. They explained that special hardware design can improve processing time and achieve better performance per unit silicon area. Theoretical and experimental results are presented to prove architectural effectiveness of FPGA [8].
Moussa et al. stated that Artificial Neural Networks are parallel architectures suitable for implementation on FPGAs. An important application problem is to determine the numerical precision formats that establish the appropriate balance between precision and the application area. Standard single or double digit precision representations require significant hardware resources while minimizing quantization errors [9]. When the structure of FPGA development cards is analyzed, it is seen that different elements other than FPGA are used. Some FPGAs may include special blocks such as multiplexers, DSPs and microprocessors. After the blocks of Complex Programmable Lagic Devices are configured, the structure cannot be restored to its original state, so they are used with erasable and writeable memory units such as EEPROM and flash. FPGAs usually use SRAM and the configuration is not permanent. This non-permanent configuration system provides free space on FPGAs and also reduces the cost as there are too many configurable arrays. The disadvantage is that it requires the use of an external Read Only Memory (ROM). FPGAs with permanent configuration are available for use in studies where no reconfiguration is required [10].

3. MATERIAL AND METHODS

Nowadays, it is known that FPGAs have high-tech varieties which can have around 1000 input-output pins and can be manufactured by using up to 9 layers with the size of nanometers. Companies like Altera, Xilinx, Atmel, Actel and Quick Logic produce FPGAs with thousands of flip-flops and millions of gates.
FPGA development cards are produced as development cards that contain various electronic devices such as memory units and various input-output and connection elements in order to program FPGAs and to check whether certain features in the written programs are working properly. In fact, these development cards are often used directly in the implementation of projects. The price range ranges from around $40 to thousands of dollars.
The units required for the production of an FPGA board which is capable of receiving and transmitting the image from the image sensor in the planned manner can be summarized as passive elements such as FPGA, input-output units, memory units, clock signaling elements, connection elements, resistance and capacitor.
The board uses EP4CE22F17C6N model numbered FPGA which has 256 pin FBGA (Fine Ball Grid Array) package structure of EP4CE22 series [11].
This device has 22320 logical elements, 594 kbit embedded memory and 66 multiplexers. FPGA was divided into 8 banks and it has 153 input/output pins. The greater number of these features in an FPGA maintains the greater design capability and simplicity to the user. Other than these, there are four general purposed PLLs (Phase Locked Loop) on this device. PLL

consists of a phase detector and an oscillator. PLL compares the phases of input signal and output signal of oscillator and maintains the overlapping. On the redesigned board, expansion pins are detected to connect the image sensor, display and several interfaces incase of need. Number of these expansion pins is three. The development board needs a 5V DC supply to operate. This power input could be applied to the 2 pinned power connection or to the first and second expansion connectors. The memory units on the board are SDRAM (Synchronous Dynamic Random Access Memory), EEPROM (Electrically Erasable Programmable Read-Only Memory) and EPCS (Serial Configuration Device). There is a 50 MHz oscillator on the board to produce the clock signal for the FPGA. Also this clock signal is used by the PLL [12].
The operation and the control of all elements on the board are subjected to the FPGA. The connections prepared between elements on the board are shown in Fig 1.

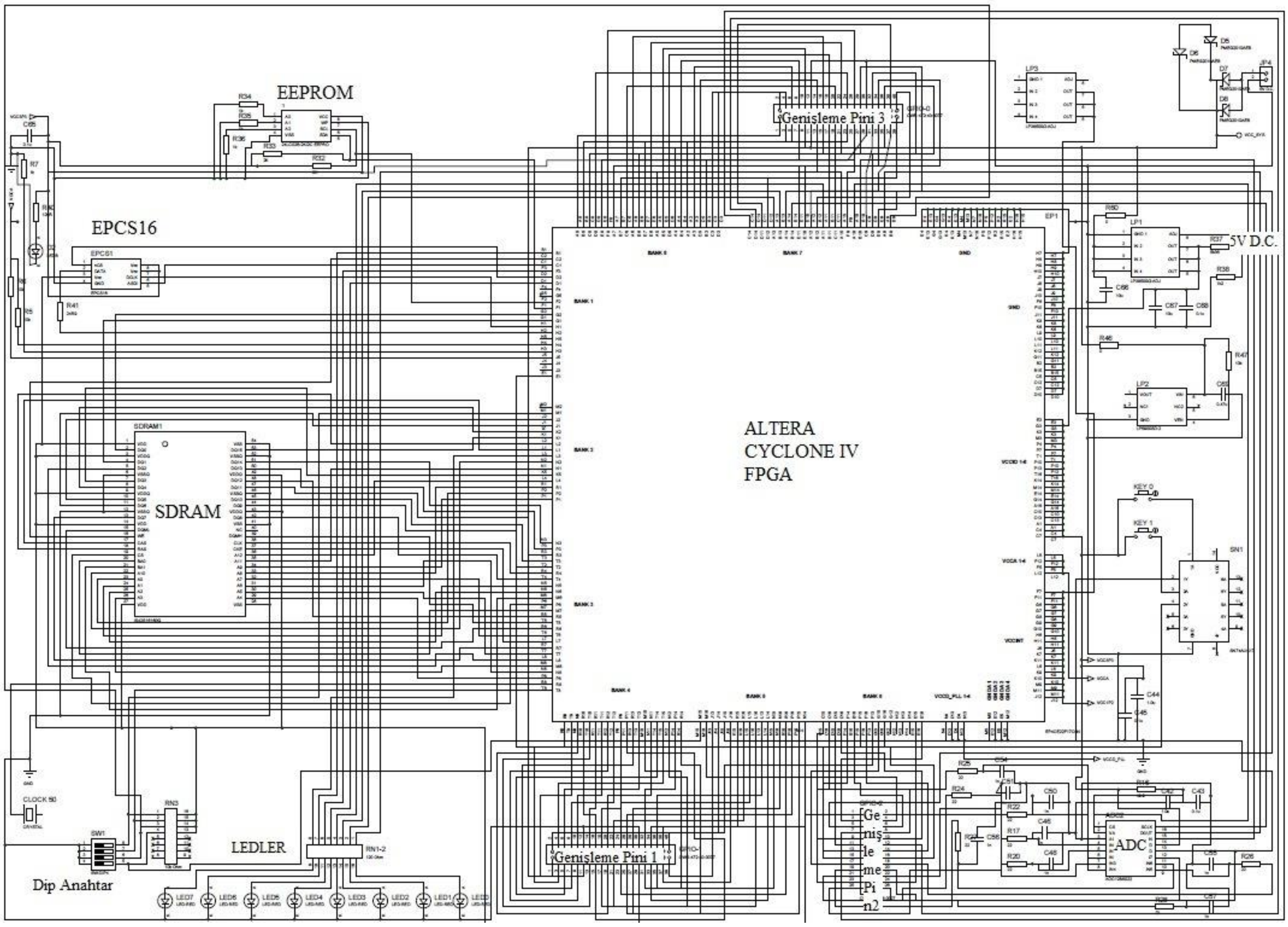


Fig. 1. *The connections prepared between elements on the board*

4. RESULT AND DISCUSSIONS

As a result of the study, updating needs for the education of engineering students was maintained with the redesign of this FPGA development board which can be used in image processing applications. Within the study a new PCB was designed and produced as in Fig 2.
In addition, an example application was carried out to work on the prepared card. In this application, the image taken from a camera in real time, displayed on the LCD in four different formats according to the positions of a dip switch. When the dip switch is in SW='X00X' position the image on the LCD shown in black and white. When it is in SW='X01X', SW='X10X' positions image is converted to grey level and red level respectively. When the switch positioned as SW='X11X' image is shown as it is get from the camera in full color [13]. These modes are shown in Fig 3.
The image comes from the image sensor to the FPGA in raw format. In the RAW2RGB module created in FPGA, there are 3 signals of 12 bits each, red, green and blue. When these incoming signals are sent to the LCD without changing, the image is displayed as color image on the screen. When converting the image from color to gray-level format, these 12-bit signals are collected and divided into 3.

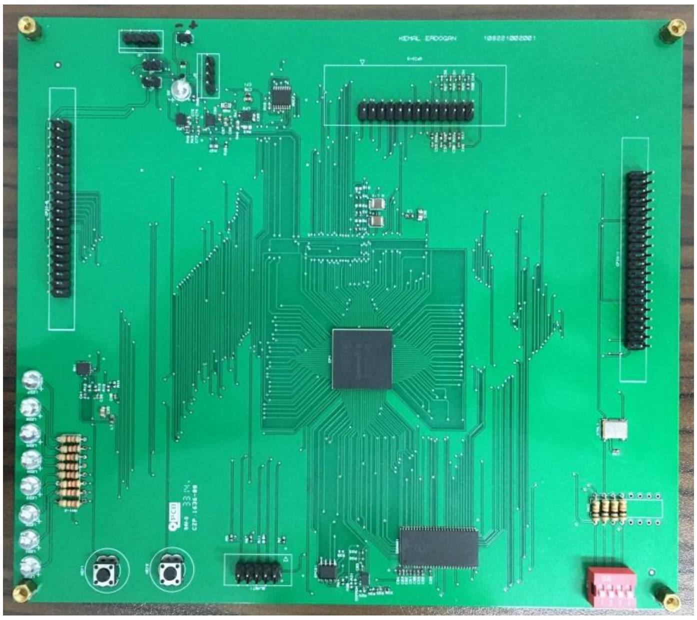
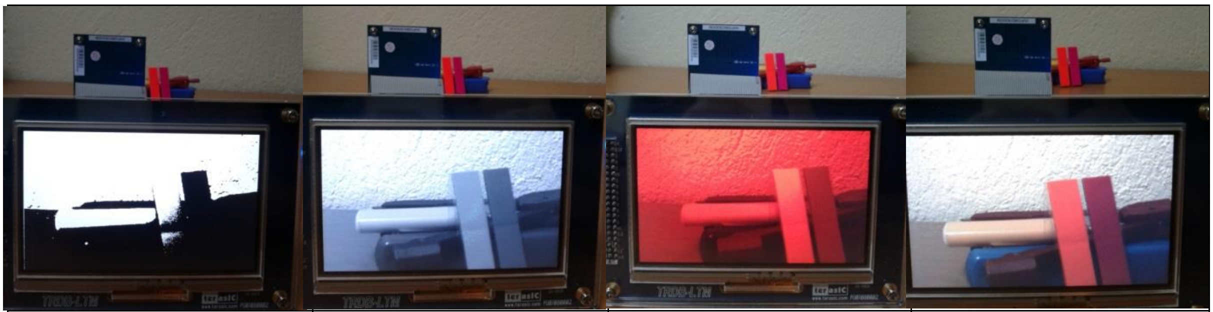


Fig. 2. *The produced board*



(a)	(b)	(c)	(d)

Fig. 3. *Real time operations on the input images: (a) black and white, (b) grey level, (c) red level and (d) full colored original.*

In other words the average of the 3 color values of the pixels is sent to the LCD for display. When the image is wanted to be displayed in black and white, all bits are sent as 1 or 0 according to the logical value of bit 12 of the average value taken. If the red-level is desired, the average value is sent only to the red signal output and the other green and blue outputs are set to 0.

With this real time image processing power, FPGA based boards are very important for the electronics engineering. In electronics engineering education simplifying of these complex boards could be important for staying update. If the boards are not too complex they could be easily updated with latest sensors or other peripheral units. Thus, education quality would not be decreased.

This study was realized to show the redesign of a complex board to a simple one is not difficult. Also this study was done for a non-commercial aim. As a future work similar boards could be used for student projects about real time image processing applications and the comparisons could be done.

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