

Investigation of Power Consumption Effect of Various Memristor Emulators on a Logic Gate

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ABSTRACT

Memristor, also known as memory resistor, is considered as the fourth passive electronic element expressing the relationship between magnetic flux and electric charge. One of the most important features of the memristor is that it has low power consumption. Minimizing power consumption is an important issue in the electronic circuits. However, the fact that the memristor element was not yet fully manufactured has led researchers to design memristor-like emulator circuits. These circuits, which approximate the memristor properties, are realized by combining the other existing electronic elements. In this paper, a basic NAND logic gate is considered and the change in power consumption when using a memristor instead of the standard resistor in the gate circuit is examined. For this purpose, the NAND logic circuit was constituted for four different memristor emulators, and the power consumption values of these circuits were obtained by simulation and experiments. These values are compared with the power consumption values of NAND circuits obtained by using standard resistors equivalent to the memristor resistance. The results clearly show that the memristor gate circuits reduce power consumption compared to standard resistive gate circuits.

1. INTRODUCTION

The basic electrical variables of circuit theory are defined as voltage, current, electric charge and magnetic flux. Considering the relationships between these variables, Professor Leon O. Chua of Berkeley University in 1971 reported that the relationship between electric charge and magnetic flux was missing. Since it is not possible to overcome this deficiency with different combinations of existing elements such as resistor, capacitor and inductor, he introduced a new element called *memristor* and defined its electrical behavior as *memristance* [1]. With this discovery, all the interrelationships between four basic electrical variables were revealed, as shown in Fig. 1. However, Chua was not able to directly obtain the memristor element in those years due to the lack of possibilities and therefore he designed an emulator circuit that approached the role of memristor. In the following years, Chua continued his work on memristor such as the description of memristive systems [2], modeling of various circuits using memristor and other nonlinear circuit elements [3], etc. Other researchers have also made various contributions to the literature on memristor. Definition of the bond-graph model of the memristor [4], analysis of nonlinear circuits containing memristor [5], dynamical analysis of the memristive diode model [6], expression of memristor with

inverse Lagrangian equations [7], the design of an alternative memristive diode model [8], the definition of the resistance switching behavior that can be reproduced in thin oxide films whose hysteresis structure properties resemble the hysteresis of the memristor [9], and the use of memristive nano devices in pattern recognition [10] can be listed as the studies. All of them are theoretical studies on the memristor [11]. In 2008, a group of researchers from HP laboratories announced that they modeled the memristor using titanium dioxide doped with oxygen and physically obtained it [12,13]. With the modeling of the memristor, the interest on the subject has gained an increasing attention on the areas of electrical circuits [14,15], computer memory architectures [16], neuromorphic devices [17], chaotic systems [18,19], and so on.

Memristor element is not yet an element commercially available in the electronics market due to its high cost and stability problems. This has led researchers to design different emulator circuits that can serve as a memristor. One of these studies is a memristor emulator circuit formed using a differential amplifier, an integrator, an analog multiplier and some passive elements [20]. In the circuit, since the analog multiplier expresses the product of the current and the charge, the output of the emulator is nonlinear. Another is a memristor emulator presented by Muthuswamy and designed using an




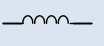


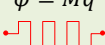
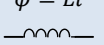
	Electrical charge (q)	Current (i)	Voltage (v)	Magnetic flux (φ)
Electrical Charge (q)	-	$q = \int i dt$	Capacitance $q = Cv$ 	Memristance $q = \varphi/M$ 
Current (i)	$i = dq/dt$	-	Resistance $i = v/R$ 	Inductance $i = \varphi/L$ 
Voltage (v)	Capacitance $v = q/C$ 	Resistance $v = Ri$ 	-	$v = d\varphi/dt$
Magnetic Flux (φ)	Memristance $\varphi = Mq$ 	Inductance $\varphi = Li$ 	$\varphi = \int v dt$	-

Figure 1. Basic linear electronic components and their relations.

analog multiplier, an integrator op-amp, a derivative op-amp and some passive elements [21]. In another study, Alharbi *et al.* designed a current controlled emulator with an exponential amplifier and an integrator using a second generation non-inverting current conveyor (CCII+). In the circuit, the exponential amplifier is used to provide the nonlinearity required for memristive behavior [22]. Another emulator circuit proposed by Alharbi *et al.* has voltage controlled feature and consists of AD844 operational amplifier and analog multiplier elements [23]. In addition to these emulator circuits mentioned, there are also many different emulator circuits in the literature (for more details, see [11] and [24]).

In this study, a NAND gate is considered in order to investigate the logic gate power consumption performances of some memristor emulators proposed in the literature. For comparison, four different emulator circuits are used as memristor. The power values consumed in each circuit built with memristor emulators are determined. Then, the power consumption of the gate circuits using standard resistance equivalent to the memristance value of the memristor emulator is examined. The power consumption values of the NAND gate using memristor emulators and also standard resistors selected as equivalent to the memristance of emulators are compared. As a result, it is clearly seen that using memristor instead of standard resistor in the NAND gate results in lower power consumption. To the best of the authors' knowledge, no previous attempt has been made to compare the performance of these emulators in logic applications in this way. Therefore, the main contribution of the study to the literature is to show that the memristor can be used in logic circuits in terms of lower power consumption. This gives an idea that the use of memristor in electronic circuits and computer systems will lead to more advantageous results in the future.

2. BASIC PROPERTIES OF MEMRISTOR ELEMENT

The memristance of a memristor is defined by

$$M(q(t)) = \frac{d\varphi(t)}{dq(t)} \quad (1)$$

where M represents the memristance, φ is the magnetic flux and q is the electrical charge. So, as can be understood from Eq. (1), the memristor is expressed by the ratio of magnetic flux to electrical charge. The differential expression can be arranged as

$$M(q(t)) = \frac{d\varphi/dt}{dq/dt} = \frac{v(t)}{i(t)}. \quad (2)$$

From Eq. (2), it is seen that the expression of memristance is similar to the ohm law in resistance, but its value changes depending on the amount of charge flowing through it. Therefore, memristor is a circuit element whose memristance decreases when the current is applied from one direction, and its memristance increases when applied in the opposite direction. If the current applied to the element is interrupted, the charge transfer on it stops. However, when the current is applied again, the charge flow continues where it left off. Because of this feature, memristor is also defined as a memory resistor. As mentioned above Chua proved that the new element will generate voltage from current like a resistor, but this voltage will show a more complex and dynamic change depending on the voltage build-up with the change of current and magnetic flux as a result of the movement of the charge (Fig. 2). As shown in Fig. 2, if the memristance of a memristor characterized by a differential load controlled φ - q curve has a non-negative value, that is $(q) \geq 0$, then the instantaneous power of the element has given as

$$P(t) = M(q(t))(i(t))^2. \quad (3)$$

The power will be positive from Eq. (3) and therefore the memristor will show the passive element characteristics [1].

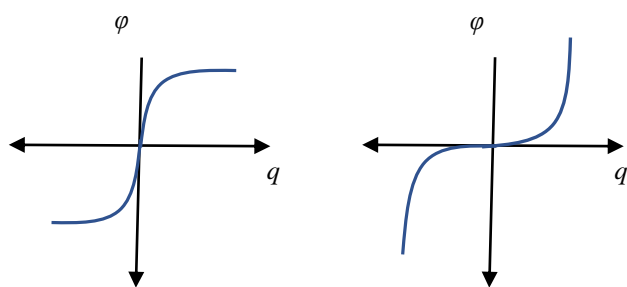


Figure 2. φ - q curves of a memristor [1].

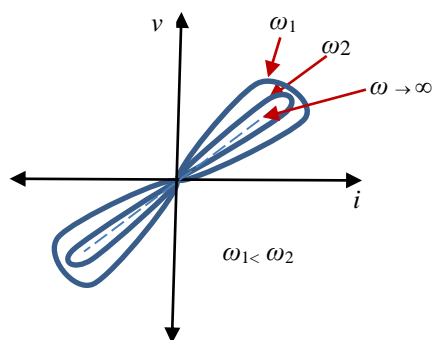


Figure 3. v - i characteristic of a memristor [2].

Continuing their memristor research, Chua and his team proved in their subsequent research that the current-voltage characteristic of a memristor, as seen in Figure 3, exhibits a hysteretic property in the form of a two-leaf clover that changes according to the frequency value applied to the element [2]. As the frequency increases, the hysteretic field narrows and when it approaches infinity, the characteristic resembles the linear resistance characteristic. According to the i - v characteristic, the memristor can have many memristance values varying within a limited range. When the current flowing through the memristor is zero, the voltage is also zero, i.e. there is no phase difference and thus no energy is stored on the memristor. This is a result of the pinched hysteretic feature. Including this feature of the memristor in his work in 1980, Chua summarized some characteristic properties of the memristor as follows [3]:

- Under very high frequency periodic large signal current excitation, the memristive element is equivalent to a linear resistor whose resistance depends on the initial state $x(0)$ which gives rise to the periodic voltage response.
- A passive memristive element can only dissipate energy; that is, it cannot store energy for later recovery.
- Any voltage-current signal pair of a single port memristive element must pass through the zero point in the same time period.
- The memristive element is passive for every $(x,i) \in R^{(n+1)}$ only if $R(x,i) > 0$.

3. MEMRISTOR EMULATOR CIRCUITS

The circuits that provide the characteristic features of the memristor and consist of different electronic elements are called *memristor emulator circuits*. In the literature, many memristor emulator circuits have been designed using different methodologies and topologies, and some of them are mentioned in Section 1. The first of these is an analog memristor emulator designed by Chua in 1971 [1].

In this section, four memristor emulators chosen from the literature will be simulated and installed in the laboratory, then the graphs of the hysteretic current-voltage characteristics will be presented. Thus, it will be checked whether each emulator generates the desired memristor characteristics or not.

3.1. Memristor emulator designed by Mutlu-Karakulak

The memristor emulator presented to the literature by Mutlu and Karakulak consists of a differential amplifier, an integrator, an analog multiplier, a diode and seven resistors [20]. The emulator circuit was established in the Multisim program and the desired current-voltage characteristic was obtained as a result of the simulation. The memristance value of the emulator is determined as 24.49 k Ω . It has been observed that when the frequency is reduced in the circuit, the leaves of the hysteresis curve expand, when the frequency is increased, the hysteresis curve becomes narrower and at very high frequencies the hysteresis curve turns into a standard resistance characteristic. In order to verify the simulation results, the circuit was also set up in the laboratory and it was verified that the desired hysteresis properties were achieved. Experimentally, the memristance value of Mutlu and Karakulak emulator was obtained as 23.405 k Ω . The experimental and simulation results of the Mutlu-Karakulak memristor emulator are given in Fig. 4, and the usability of this emulator in both experimental and simulation environments has been revealed.

3.2. Memristor emulator designed by Muthuswamy

The emulator circuit proposed by Muthuswamy, a student of Chua, is a circuit designed specifically to use in chaotic circuits and has more nonlinear properties [21]. The emulator consists of two analog multipliers, an integrator, a differential amplifier and some resistors. The multisim schema of this memristor emulator is shown in Fig. 5. According to the simulated results, the memristance value of the emulator is 25.23 k Ω , while the experimental memristance value is 20.5 k Ω . As can be seen from Fig. 5, it was observed that the memristor emulator designed by Muthuswamy provided the necessary characteristics.

3.3. Current controlled memristor emulator designed by Alharbi et al

Alharbi *et al.* presented a current controlled memristor emulator to the literature [22]. The simulation circuit of the emulator and the hysteresis curve are obtained in Fig. 6. According to the simulation results, the memristance value of the circuit was found to be approximately 2.5 k Ω . Increasing frequencies values are also applied to the circuit and it has been observed that the leaves gradually contract at high frequencies, which are a memristor feature. The hysteresis curve of the current-controlled emulator implemented in the laboratory is also given in the Fig. 6. The memristance value of the emulator is 2.3 k Ω . According to the experimental results obtained from the implemented circuit, the necessary memristive properties are provided.

3.4. Voltage controlled memristor emulator designed by Alharbi et al

Another memristor emulator is the voltage controlled circuit designed by Alharbi *et al.* [23]. Based on the operational amplifier, second generation current conveyors and analog multiplier, this circuit is advantageous in that it is a low-element memristor emulator. The simulation diagram of the circuit and the current-voltage characteristics obtained

from simulation and experimental results are given in Fig. 7. According to the simulation results, the memristance value of the emulator is approximately 1.38 kΩ. According to the data obtained in the laboratory, the memristance value of the

emulator is 1.33 kΩ. It has also been observed that when the frequency is increased more, the hysteresis curve becomes narrower.

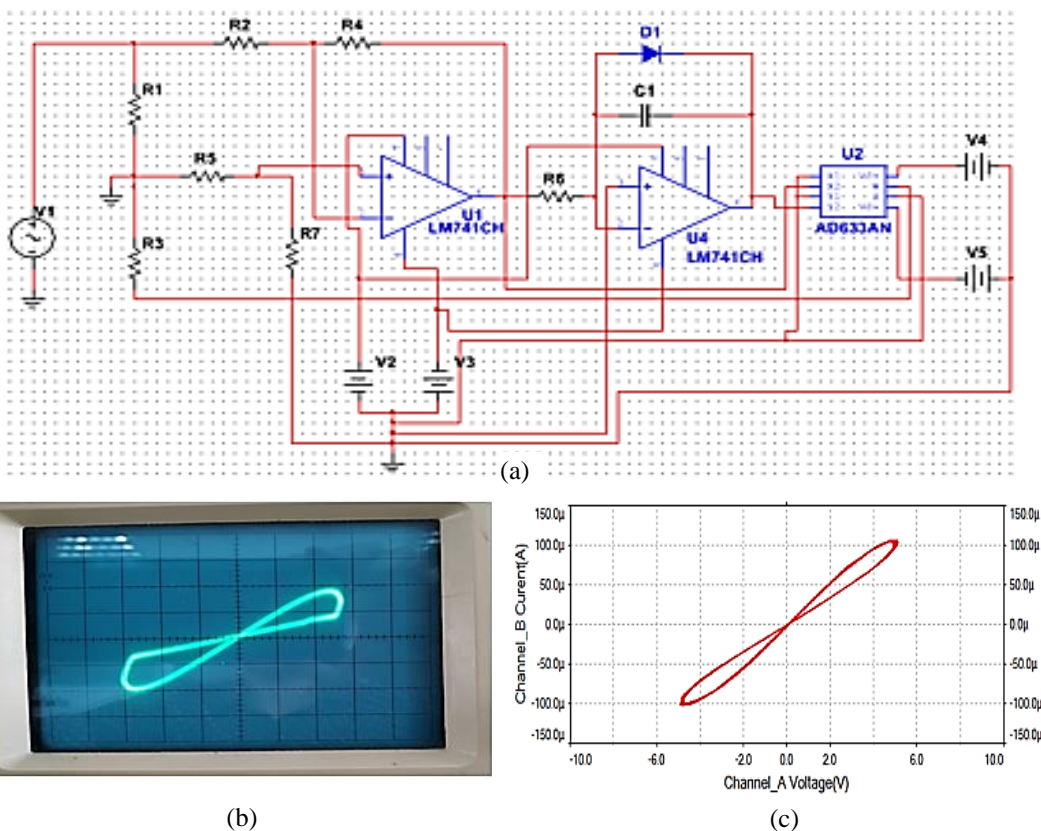


Figure 4. Mutlu-Karakulak's memristor emulator: Simulation circuit (a)- experimental *i-v* characteristic (b)-simulation *i-v* characteristic (c).

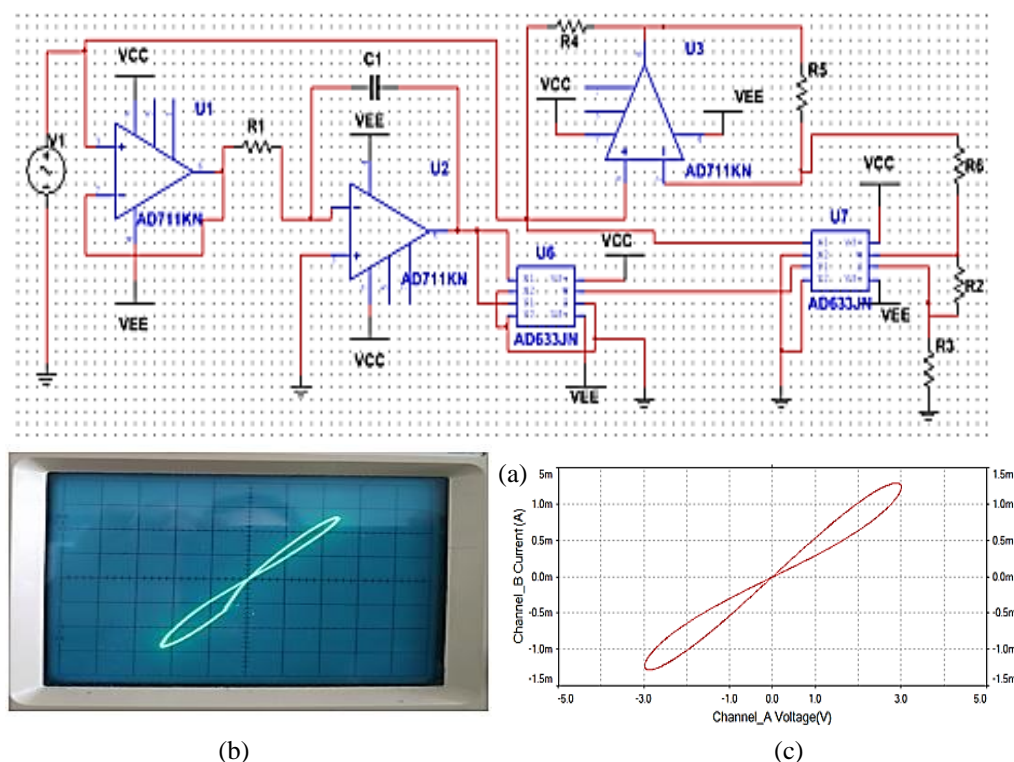


Figure 5. Muthuswamy's memristor emulator: Simulation circuit (a)- experimental *i-v* characteristic (b)-simulation *i-v* characteristic (c).

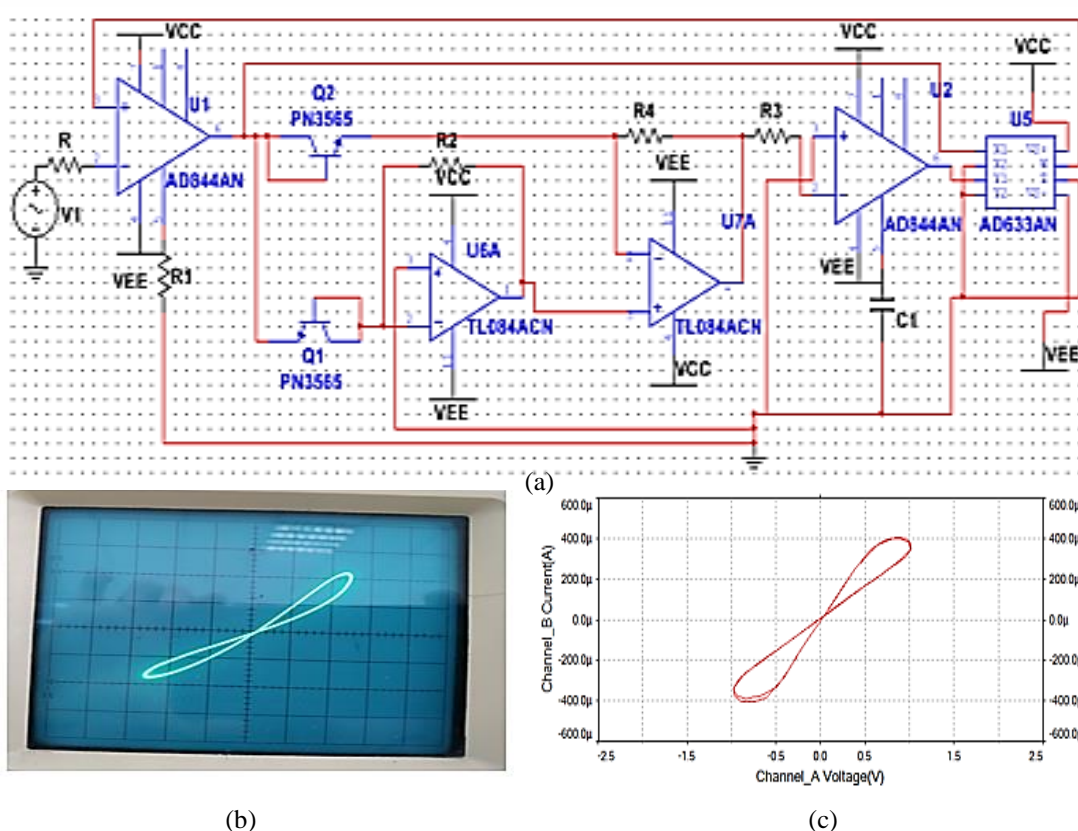


Figure 6. Alharbi *et al*'s current controlled memristor emulator: Simulation circuit (a) - experimental *i-v* characteristic (b)-simulation *i-v* characteristic (c).

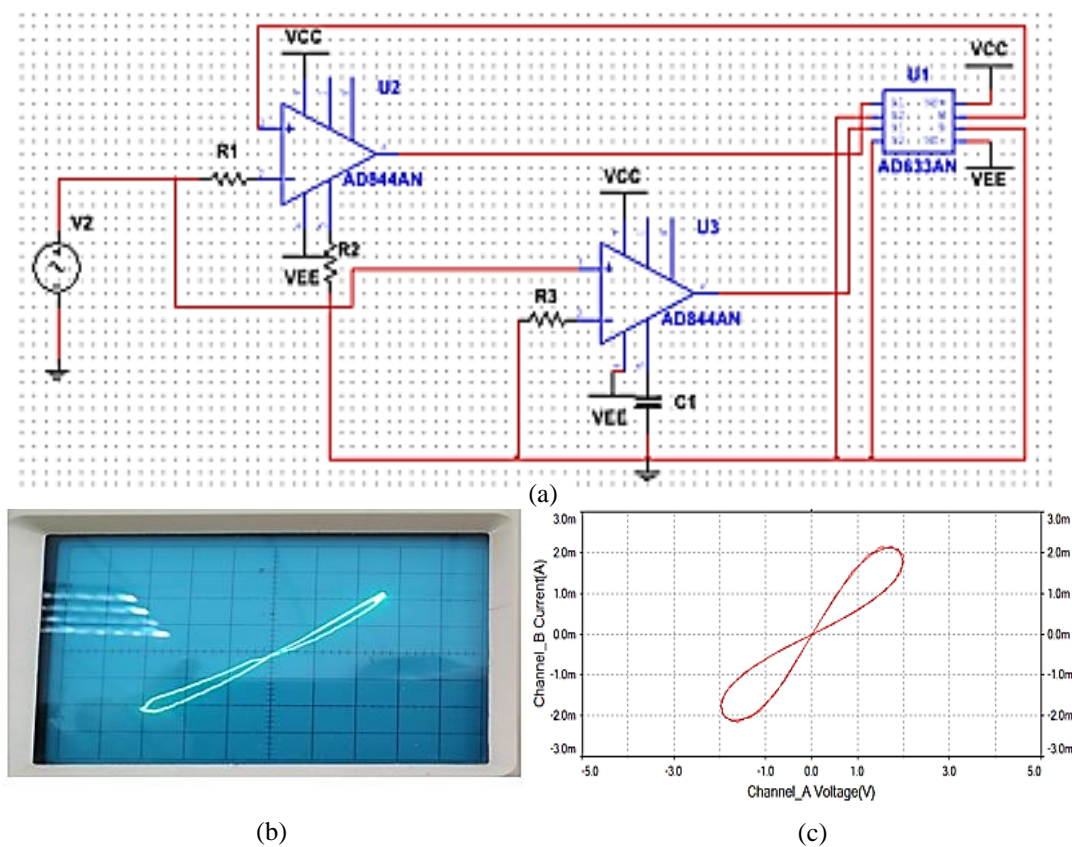


Figure 7. Alharbi *et al*'s voltage controlled memristor emulator: Simulation circuit (a) - experimental *i-v* characteristic (b)-simulation *i-v* characteristic (c).

4. NAND LOGIC GATE WITH MEMRISTOR EMULATOR

Logical gate circuits produce logical results that match the input data in a given Boolean Algebra framework. These logic gates have many features such as speed, noise immunity, power consumption, output capacity, input capacity, supply voltage, propagation delay, logic voltage levels and so on. A good logic integration should consume little power, work fast, be low cost and be less sensitive to environmental conditions [25]. Therefore, power consumption is an important consideration for a designer. The amount of power consumed in a logic gate is related to the average of the currents drawn by the gate output in the logic 0 and logic 1 states. The logic zero value has to be taken into account because in this logic case there is also power consumption. The current drawn from the supply of a logic gate is obtained in the form of

$$I_{logic} = 0.5(I_{logic\sim 0} + I_{logic\sim 1}). \quad (4)$$

where $I_{logic\sim 0}$ denotes the current drawn when the logic gate output is 0 while $I_{logic\sim 1}$ represents the current drawn when the logic gate output is 1. The power taken from the supply source (P) is obtained as the product of the supply voltage (V_{logic}) and the current drawn from the supply (I_{logic}) as follows

$$P = V_{logic} \times I_{logic}. \quad (5)$$

where V_{logic} given in Eq. (5) is the source feed of the gate.

In this study, a NAND gate is considered to examine the usability of memristor in terms of power consumption in logic gates. The NAND gate is preferred because it has an internal circuit structure that contains more elements than classical AND and OR gates. In Fig. 8, a traditional NAND circuit with MOSFETs and its new version obtained by using a memristor instead of R resistor in the circuit is given.

In the emulator circuits seen in Figs. 4-7, the terminals of the voltage sources are used as the terminals of the memristor to be connected instead of the resistance in the gate circuit.

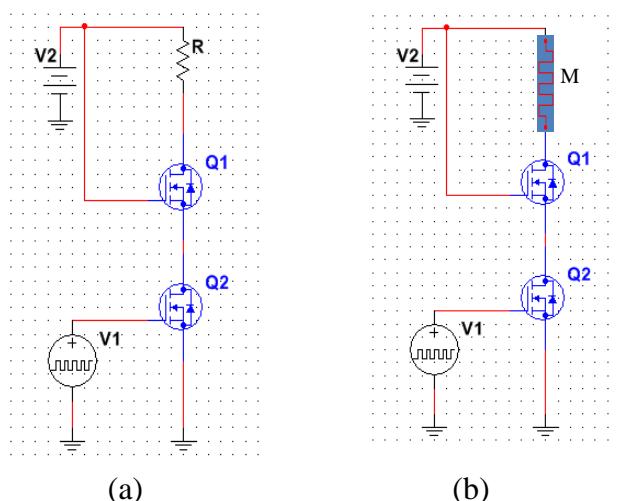


Figure 8. NAND logic gate with standard resistor (a) and with memristor (b).

The comparison of the power consumed by the NAND gates containing the emulator of Mutlu and Karakulak, and the containing the standard resistor equivalent to the memristor of the emulator is given in Fig. 9. Similarly, the power consumption data of NAND circuits obtained using the emulators of Muthuswamy and Alharbi *et al.* and using resistors equal to the memristances of these emulators are shown in Figs. 10-12, respectively. In these figures, the average values of the input voltage, the current drawn from the source and the power consumption values obtained according to Eq.(4) are shown. The simulated and experimental results of power consumption values for four different memristor emulators and their equivalent standard resistors are given in Tables 1 and 2. According to the simulation results given in Table 1, the logic gate using Mutlu-Karakulak memristor emulator consumed 41.67% less power than the logic gate using standard resistor. The logic gate in which Muthuswamy memristor emulator is used consumes 33.33% less power than the standard resistive logic gate. Similarly, the logic gate in which the Alharbi *et al* current-controlled memristor emulator is used consumes 41.04% less power than the standard resistive logic gate. Finally, the logic gate using the Alharbi *et al* voltage-controlled emulator, consumes 10.11% less power than the standard resistive logic gate. According to the experimental results given in Table 2, the logic gate using Mutlu-Karakulak memristor emulator consumed 25.00% less power than the logic gate using standard resistor. The logic gate in which Muthuswamy memristor emulator is used consumes 32.14% less power than the standard resistive logic gate. Similarly, the logic gate in which the Alharbi *et al* current-controlled memristor emulator is used consumes 32.33% less power than the standard resistive logic gate. Another comparison, the logic gate using the Alharbi *et al* voltage-controlled emulator, consumes 25.25% less power than the standard resistive logic gate. From these tables, it is clear that for each pair of memristor emulator-resistor, the memristive NAND gate consumes less power than the classical resistive NAND gate. This result shows that it is more advantageous to use memristor instead of classical resistor in logic circuits where low power consumption is important. Thus, it can be thought that the memristor element will be widely used in the industry when it is commercially available in the future.

5. CONCLUSIONS

In this study, the advantages of using memristor for low power consumption in logic circuits are investigated. In a NAND logic gate, the memristor emulator representing the memristor element is used instead of the standard resistor. Four different memristor emulators were considered, namely Mutlu-Karakulak, Muthuswamy, Alharbi *et al*'s current-controlled and voltage-controlled emulators. Firstly, memristive properties of emulators were obtained by experimental and simulation. Later, these emulators were connected instead of the standard resistor of the NAND gate and their power consumption was examined. Accordingly, all four emulators were found to have less power consumption than standard resistors. The results obtained by using memristor in this study can lead to new research areas by taking into account memory-based speed, power quality factor and similar features for future studies.

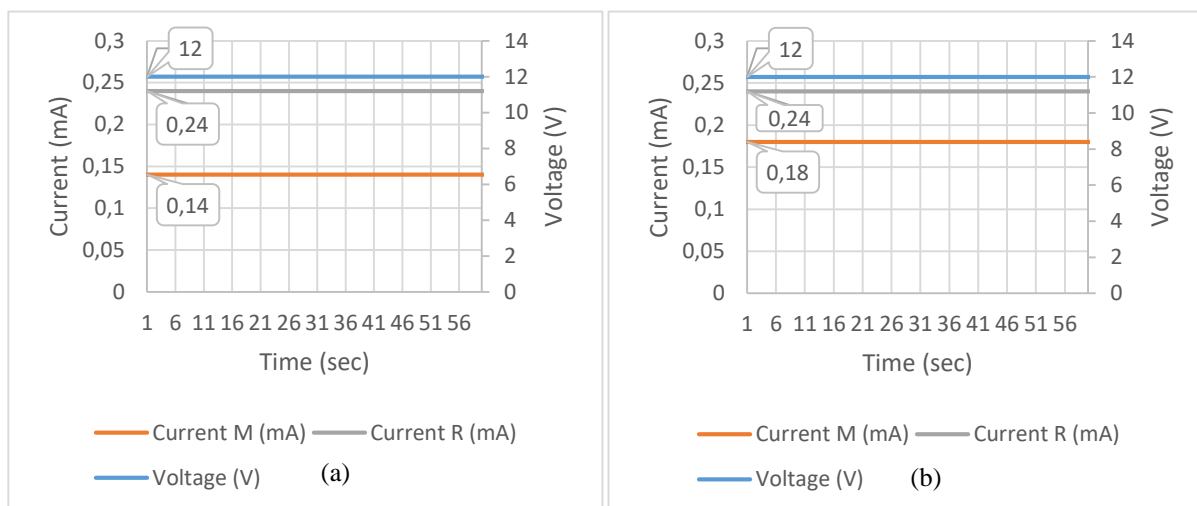


Figure 9. Simulation (a) and experimental (b) results of current-voltage values consumed by NAND logic gate with standard resistor and Mutlu-Karakulak emulator

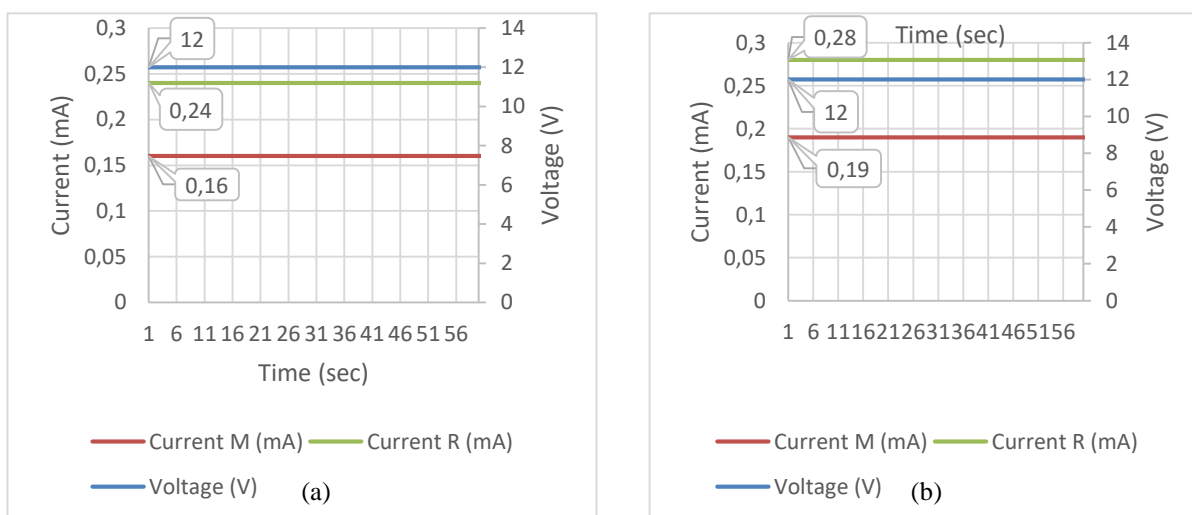


Figure 10. Simulation (a) and experimental (b) results of current-voltage values consumed by NAND logic gate with standard resistor and Muthuswamy emulator.

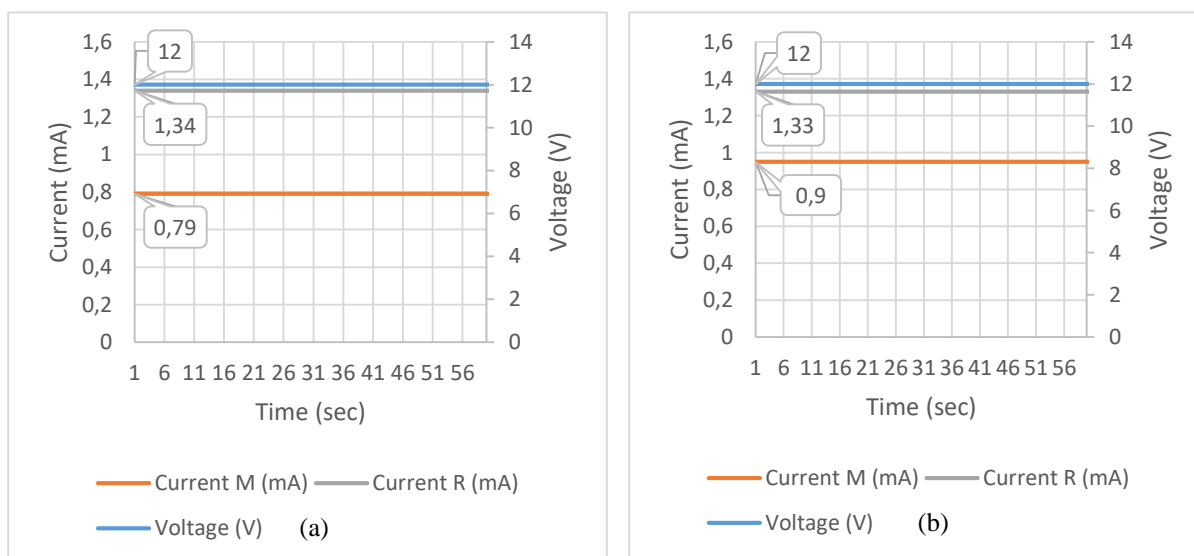


Figure 11. Simulation (a) and experimental (b) results of current-voltage values consumed by NAND logic gate with standard resistor and Alharbi *et al* current controlled emulator.

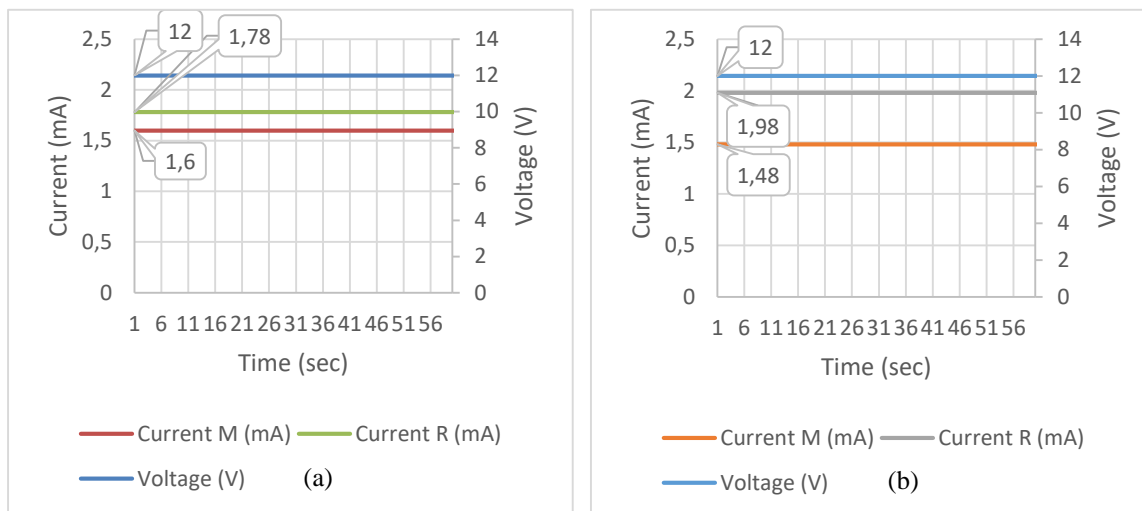


Figure 12. Simulation (a) and experimental (b) results of current-voltage values consumed by NAND logic gate with standard resistor and Alharbi *et al* voltage controlled emulator.

TABLE 1. SIMULATED LOGIC CIRCUITS; VOLTAGE, AVERAGE CURRENT AND POWER VALUES

Logic Circuits	Voltage (V)	Average Current (μ A)	Power (mW)	Memristor's Power Minimization
NAND gate with Mutlu <i>et al</i> emulator ($M=24.49$ k Ω)	12	140	1.68	%41.67
NAND gate with resistance equivalent to Mutlu <i>et al</i> emulator ($R=24.49$ k Ω)	12	240	2.88	
NAND gate with Muthuswamy emulator ($M=25.23$ k Ω)	12	160	1.92	%33.33
NAND gate with resistance equivalent to Muthuswamy emulator ($R=25.23$ k Ω)	12	240	2.88	
NAND gate with Alharbi <i>et al</i> current controlled emulator ($M=2.5$ k Ω)	12	790	9.48	%41.04
NAND gate with resistance equivalent to Alharbi <i>et al</i> current controlled emulator ($R=2.5$ k Ω)	12	1340	16.08	
NAND gate with Alharbi <i>et al</i> voltage controlled emulator ($M=1.38$ k Ω)	12	1600	19.2	%10.11
NAND gate with resistance equivalent to Alharbi <i>et al</i> voltage controlled emulator ($R=1.38$ k Ω)	12	1780	21.36	

TABLE 2. EXPERIMENTAL LOGIC CIRCUITS; VOLTAGE, AVERAGE CURRENT AND POWER VALUES

Logic Circuits	Voltage (V)	Average Current (μ A)	Power (mW)	Memristor's Power Minimization
NAND gate with Mutlu <i>et al</i> emulator ($M=23.4$ k Ω)	12	180	2.16	%25.00
NAND gate with resistance equivalent to Mutlu <i>et al</i> emulator ($R=23.4$ k Ω)	12	240	2.88	
NAND gate with Muthuswamy emulator ($M=20.5$ k Ω)	12	190	2.28	%32.14
NAND gate with resistance equivalent to Muthuswamy emulator ($R=20.5$ k Ω)	12	280	3.36	
NAND gate with Alharbi <i>et al</i> current controlled emulator ($M=2.3$ k Ω)	12	900	10.8	%32.33
NAND gate with resistance equivalent to Alharbi <i>et al</i> current controlled emulator ($R=2.3$ k Ω)	12	1330	15.96	
NAND gate with Alharbi <i>et al</i> voltage controlled emulator ($M=1.33$ k Ω)	12	1480	17.76	%25.25
NAND gate with resistance equivalent to Alharbi <i>et al</i> voltage controlled emulator ($R=1.33$ k Ω)	12	1980	23.76	

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