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Original Research Article

SPICE modelling and analysis of hybrid energy harvester combiner topologies

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David Selvakumar *, Mervin J, Anurupa Ghosh, Arnab Deb

Secured Hardware and VLSI Design Group, Centre for Development of Advanced Computing (C-DAC), Bangalore, India

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* Corresponding author
david@cdac.in

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ABSTRACT

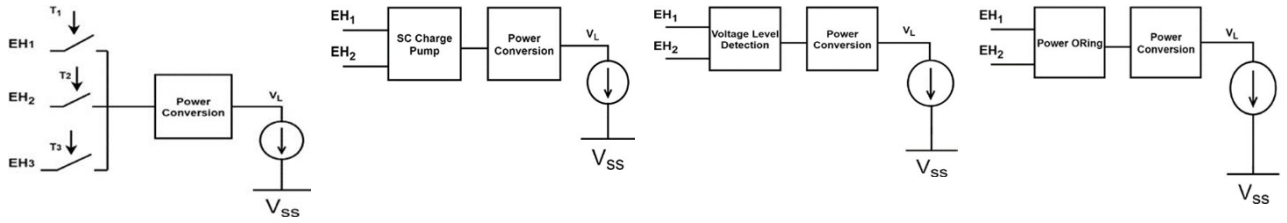
Harvesting energy from multiple hybrid sources and efficiently combining the harvested energies is critical for enabling self-powered devices. Designing an efficient energy combiner is a technical challenge and is non-trivial. Various factors viz. kinds of sources, harvestable energy level and range from the sources, electrical characteristics of sources (low current and high voltage, high current and low voltage, capacitive, inductive etc.), impedance matching (resistive, resistive-reactive, modulus, complex conjugate etc.) of sources, sources scheduling algorithms for combiner, sources switching and control/trigger circuit losses, power conversion and management etc. influence the overall energy combiner's efficiency. Considering that, this article presents a SPICE modelling and simulation framework for analyzing hybrid energy harvester combiner topologies such as Inductor sharing, voltage level detection and powerORing for its power and energy flow characteristics, regulation, and energy combining efficiency. Such analysis through simulation enables arriving efficient combiner architecture for the chosen harvestable resources, source models, power management circuits and schemes etc. Based on a case study with three different kinds of sources, it has been observed that the voltage level detection technique with DC-DC converters results in the highest efficiency as compared with the other two topologies for such a scenario.

Keywords: Energy combiner modelling; Hybrid sources energy harvesting; Inductor sharing; PowerORing and voltage level detection; SPICE modelling and simulation

1. Introduction

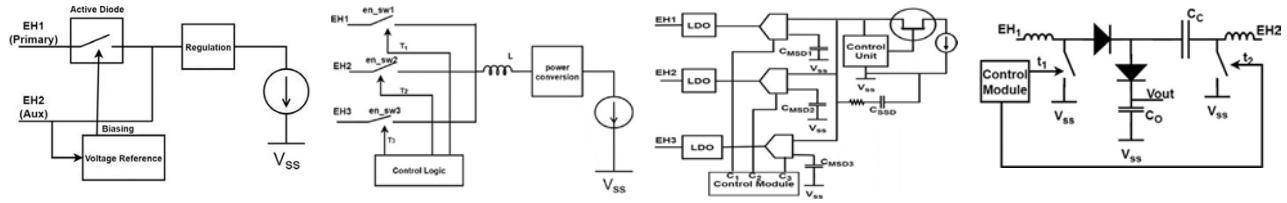
Self-powered autonomous devices do sensing, processing, communication, and actuation. Perpetual operation of such systems demands energy harvesting from residual ambient power sources [1-3], efficient energy extraction and conversion, efficient power management [1] and storage. [4] focuses on modelling, simulation, and analysis of the practical feasibility of a dual piezo harvester (PZ) to power a wireless sensor end device. Considering that it is impractical to adopt a single source-based harvester to power perpetual devices, combining energy from multiple sources (same or different types) efficiently is the key and is not trivial. Many research works have illustrated this and [3,9] and [23] consolidate and present as surveys. Due to the differing characteristics of multiple sources, an efficient power extraction, conversion, management, combiner, and storage circuits to achieve higher overall system efficiency is essential. High conversion efficiency across all the stages is important and is influenced by numerous parameters. Considering this, a SPICE simulation and analysis framework to model and evaluate various energy combiner topologies with transducer and power converter models is needed. PowerORing, voltage level detection, complementary use of converters/energy sources, Inductor sharing across multiple converters/sources, time multiplexing the input sources, multi-input combining with a switched capacitor, multi-input boost converter and multi-input combining with linear regulators etc. are a few energy combining techniques. This article focuses on a generic SPICE modelling, simulation, and analysis of PowerORing

[5-10], Voltage Level Detection [11-15] and Inductor sharing [20-22] energy combiner topologies on the aspects of power/energy consumption, impedance matching (resistive and modulus, switching frequency), energy efficiency etc. with source transducer's (Thermoelectric (TEG), Photovoltaic (PV) and Piezoelectric (PZ)) & power converter's static analytical models. Other techniques presented in [17-20] viz. Complementary use of Energy Source, Multi-Input (Dual) Switched Capacitor and Multi-Input Boost Converter Topology etc. are not addressed in this article. Figures 1 and 2 present the schematics of energy combiner techniques [9,23]. The objective of this work is to develop a SPICE modelling and simulation framework for analyzing Hybrid Energy Harvester (HEH) combiner topologies viz. Inductor sharing, voltage level detection and powerORing for its power and energy flow characteristics, regulation, and energy efficiency to enable arriving at an efficient combiner architecture based on harvestable resources, sources models, power management circuits, schemes etc. As a case study, we have evaluated the framework with three different kinds of sources and observed that the voltage level detection technique with a DC-DC converter gives the highest efficiency as compared with other topologies viz. Inductor sharing and powerORing. We haven't come across any work on such modelling and simulation frameworks for simulating and analyzing various HEH and HEC topologies with the various energy source models.



(a) Time multiplexing (b) Schematic of switched capacitor charge pump (c) Schematic of voltage level detection (d) Schematic of PowerOring

Fig. 1. Energy combiner techniques [9]



(a) Schematic of complementary use of sources (b) Schematic of inductor sharing (c) Schematic of multi-input boost converter (d) Schematic of multi-input combining with linear regulators

Fig. 2. Energy combiner techniques [23]

The structure of this paper is as follows: Section II presents the design basis and goals for hybrid energy harvester (HEH) and hybrid source energy combiner (HEC) circuits. Section III depicts the building blocks of HEH and the significance of each. Section IV presents the electrical characteristics of energy sources and the electrical equivalent circuits/ parameters adopted in this work for SPICE simulation and analysis. Section V analyzes the various published research works on HEC circuit topologies viz. powerORing, inductor sharing, voltage level detection and variants thereof, and impedance matching of sources for deriving the parameters to be considered for SPICE simulation and analysis. Section VI elaborates on the SPICE models for the above combiner topologies. Section VII presents a modelling viability comparison and analysis between our SPICE simulation models and the combiner topologies cited in the references. Section VIII concludes and presents future works.

2. Material and Methods

2.1. HEH and HEC – design goals and basis

An important design goal of a HEH is energy efficiency. Energy extraction from sources and combining efficiency should be high. Combiners, power management, and control circuits, clock generators, etc. should be simple and energy-efficient with low static and dynamic power dissipation. A quick self-start without any external startup is preferred. The system should be designed based on the worst-case availability of sources to provide stable power to the load irrespective of the adversities at the sources. The harvester should extract as wide a source's power range as possible and any excess besides supplying to the load should be stored in a supercapacitor or battery for reuse, a Harvest-Supply Load / Store-Use model.

2.2. HEH – building blocks and significances

The challenges in designing an energy harvesting IC include understanding the characteristics of the harvestable ambient residual sources, estimates of energy/power density retrievable from such sources, choice of transducers to harvest the sources, electrical characteristics/parameters of the transducers viz. inductive, capacitive, resistive, voltage/ current/charge/power levels, ac/dc, input, output impedances, ideal transduction efficiency etc. Depending on the need of the applications, suitable models like harvest-use or harvest-store-use or harvest-supply load/store-use need to be adopted.

A HEH can consist of the following sub-components:

1) Harvestable physical sources, the transducers that convert physical energy (thermal, kinetic, electromagnetic, photo luminance etc.) into electrical energy. The impedance matching (resistive, resistive-reactive, modulus, complex conjugate, switching frequency etc.) of physical to electrical variables and electrical parameters to load/power converters etc. are also important parameters for efficient extraction of source's energy.

2) Interface circuits (voltage multipliers, rectifiers, level shifters, resonant circuits etc.) which extract energy from the transducers and the power converters which further provide regulated outputs to loads. The power converters may be buck, boost, buck/boost with/without maximum power point tracking (MPPT) etc. The interface circuits and power converters need to have suitable impedance matching schemes to extract/ convert energy efficiently from the sources.

3) The energy combiner circuit receives inputs from various harvesters and with a suitable converter topology it combines the energy as a single voltage/current source to supply the load.

2.3. Source transducers – characteristics

TEG, PV and PZ source transducer's equivalent circuits are shown in Fig. 3 and the circuit parameters are in Table 1. The harvested voltage and input impedance values adopted for simulation are indicated in parentheses in Table 1. The desired output voltage from the energy combiner is 1.2V. For TEG and PV the impedance matching is purely resistive. For PZ sources the impedance being considered for matching is modulus impedance rather than resistive-reactive (capacitive).

Table 1. Physical and electrical parameters of sources / transducers [20]

Parameters	Thermal	Solar	Vibration
Material	BiTe	Si (1-2 in series)	PZT (1-2 in series or parallel)
Physical Variable	Temperature difference, ΔT= 2 to 5 K	Light intensity, 500-2000 lux	Acceleration >1g
Harvested Voltage (V)	0.050-0.300 (60mV)	0.2 to 0.9 (400mV)	3-10 (2.8V)
Input Impedance (kΩ)	0.005 to 0.010 (6 Ohm)	0.05 to 2 (266 Ohm)	10-150 (20KOhm) – Modulus Impedance

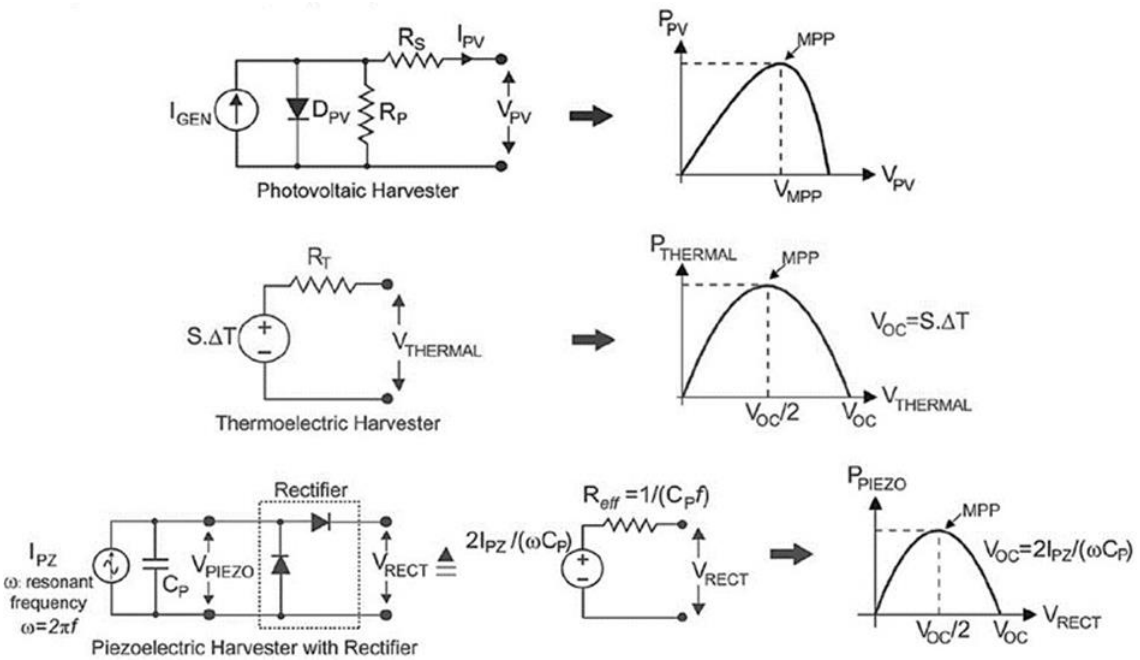


Fig. 3. Energy harvester transducer electrical models with the corresponding Max. Power Point Curves (Output Power vs Output Voltage) [20]

2.4. HEC circuit topologies – parameters for simulation and analysis

2.4.1. Power ORing

Article [5] considers photovoltaic (Avg. Power-P1) and wind (Avg. Power-P2) as HEH sources and stores the harvested energy in supercapacitors (C1 & C2) simultaneously which in turn are connected to the storage supercapacitor (C0) through Schottky diodes (powerORing). Further, storage in C0 is buck-boosted with a DC-DC converter to provide a regulated supply to load. To ensure equal/proportional contribution of both sources, C1 and C2 are suitably sized based on P1/ C1= P2/ C2. Article [6] presents an indoor dual (photovoltaic & thermal) HEH scheme with a fixed (static) "near MPPT" scheme and Schottky diodes-based combiner. Both are harvested simultaneously (no time schedule or power ratio for equal/proportional share) by a single DC-DC converter (PWM boost converter having a fixed MPPT common for both sources) and stored in a supercapacitor (energy reserve) which is further regulated by a buck dc-dc converter to deliver regulated supply to a load. The MPPT functions as a kind of impedance matching for both, even though the matching requirements of photovoltaic and TEG differ due to different Power vs. load and Power vs. Output voltage characteristics.

Article [7] details a HEH for photovoltaic and vibration, with a separate dynamic MPPT for each, powerORed with Schottky diodes and the combined energy is transferred to a supercapacitor. Neither source has separate storage. The combined energy in the single supercapacitor is regulated with a buck-boost DC-DC converter and delivered to a load. Impedance matching between power management and MPPT circuits is not illustrated.

Article [8] combines three sources viz. TEG, vibration based electromagnetic (EM) and PZ with separate power management circuits for each and combines all three DC sources as powerORed with Schottky diodes. The combiner had been realized on 180nm CMOS. The independent power management circuit for each ensures equal voltage from all three just before powerORing which enables power flow to the load from a source which has the highest harvested energy level. Articles [9, 10] consider TEG and PE harvesters, combined with active diode powerORing, and realized on 65nm CMOS. Active diode powerORing adopted in [9, 10] needs additional gate drive circuits which consume power and reduce overall efficiency. A single power management circuit for HEH conserves the area and quiescent power of the overall harvester but brings the issue of impedance matching between various sources and the power management circuit (DC-DC converter) which reduces the overall combiner efficiency.

Another drawback of powerORing is that the harvester with the highest energy will always be connected to the load and lower energy harvesters will not be utilized effectively resulting in energy leakages and reduced combiner efficiency. Further, powerORing needs more than 1V at the harvested output to overcome the diode losses. A study based on the above articles indicates that the efficiency of a powerORing combiner largely depends on, i) P-N/Schottky/Active Diode for powerORing ii) Regulated or Unregulated Voltage/Power Levels being powerORed iii) Combiner Algorithm to provide fair chances to all sources and iv) Single (shared by all sources) or Multiple power converters (one for each source).

2.4.2. Voltage level detection

Article [12] considers HEH from photovoltaic, vibration and magnetic induction-based wireless power transfer which could be classified as RF harvesting. The system is realized as an IC in 130nm CMOS. Each source has a LDO to regulate the harvested energy and store it in a single storage capacitor common for all LDO outputs and the scheme is a kind of powerORing without diodes (since the voltage levels at all LDO outputs are the same and highly regulated). Two hysteresis comparators compare the voltage level at the storage capacitor with a threshold (V*max* and V*min* provided by Band Gap Reference (BGR)) and power the load suitably with a MOSFET switch by maintaining the voltage level at the capacitor between V*max* and V*min*. Hysteresis comparators embrace voltage level detection topology. The architecture of the energy combiner proposed in [14] has a Digital control unit (DCU), comparators, storage capacitors (one each per harvested source), clock voltage doublers (CVDs) based on Dickson charge-pump, MOSFET switches and has been realized in 130nm CMOS.

Comparators compare the voltage level in storage capacitors with a threshold (same for all sources) and based on that, DCU suitably connects the sources to the load for a fixed time duration with a predefined algorithm by enabling the comparators and MOSFET switches. The scheme gives a fair chance to all the harvested sources. The combiner technique in [14] is not efficient when the energy being harvested is higher than the load requirements. Article [15] presents the HEH combiner circuit with three input source ports and two output ports viz. load (low power path (LPP)) and battery storage (high power path (HPP)) to ensure the combiner works efficiently across a wider range of input source power levels and the circuit has been realized on 130nm CMOS. The sources are connected to one of the paths depending on the power level. LPP and HPP are separately powerORed together by voltage level-based selection of sources. Depending on the input power levels the sources are either connected to LPP or HPP or switched between both. The

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control unit algorithm which is presented in [14] provides an equal chance for all the sources to deliver power to the load. Article [16] addresses the issue of combining energy from a set of homogeneous sources with widely varying power levels in each and typically with such sources, a source with the least power is generally not utilized well by the combiner. In [16], the combiner connects the harvestable sources equally and sequentially and depending on the level of energy in the source, it is either connected to the load or to a battery. Every source has an inductor-based power converter and presents a regulated/conditioned power to the combiner. A study based on the above articles indicates that the efficiency of a voltage level detection combiner hugely depends on i) the voltage references threshold scheme for the comparators ii) the frequency of schedule of the sources and iii) the energy range of the sources iv) control unit/combiner algorithm to provide equal chances to all the sources and v) Single (shared for all sources) or Multiple power converter circuits (one for each).

2.4.3. Inductor sharing topology

Article [21] presents the sharing of inductor across all the sources (piezo (with a rectifier), photovoltaic, TEG) and avoids the two-stage storage-regulation architecture for energy efficiency. The design has one primary (to load) and one secondary (storage) path, and the inductor is shared among them as well. The secondary path is invoked when the harvested energy is higher than the load requirements. When the harvested energy is less than the needs of the load, storage feeds the load through the same shared inductor buck converter. The converter operates in discontinuous conduction mode (DCM) and adopts the Zero Current Switching (ZCS) technique. The switching frequency of the converter for harvesting various sources is chosen in such a way that the input impedance of the converter matches the harvester output impedance that is being connected. Article [22] considers multiple piezo sources and a shared inductor-based converter. The internal capacitance of the piezo resonates with the inductor of the converter and energy gets transferred and subsequently inductor and output capacitor resonate, and energy is transferred to load.

Article [23] presents PV, TEG, Piezo (PZ) and RF sources-based harvester with quasi-dynamic MPPT circuit, inductor shared buck-boost converter-based energy combiner and has been realized on 320nm BCD technology. The design adopts 5V CMOS devices, low *Vt* devices and n- channel depletion MOSFET. An arbiter schedules the connection of the sources with the single power converter and serializes the access. Typically, an Inductor sharing scheme adopts a single power converter and needs interface circuits (maybe as MPPT/converter) for impedance matching of each source with the converter. [24] presents HEH with PZ and EM and adopts a single inductor for combining. Each source has a separate storage capacitor and resonates together with the single inductor for combining the energy to the load. A study based on the above articles indicates that the efficiency of inductor sharing combiner depends on i) frequency of schedule of sources ii) energy level and range of sources iii) control unit/combiner algorithm to provide fair chances to all sources and iv) efficient time utilization of shared inductor.

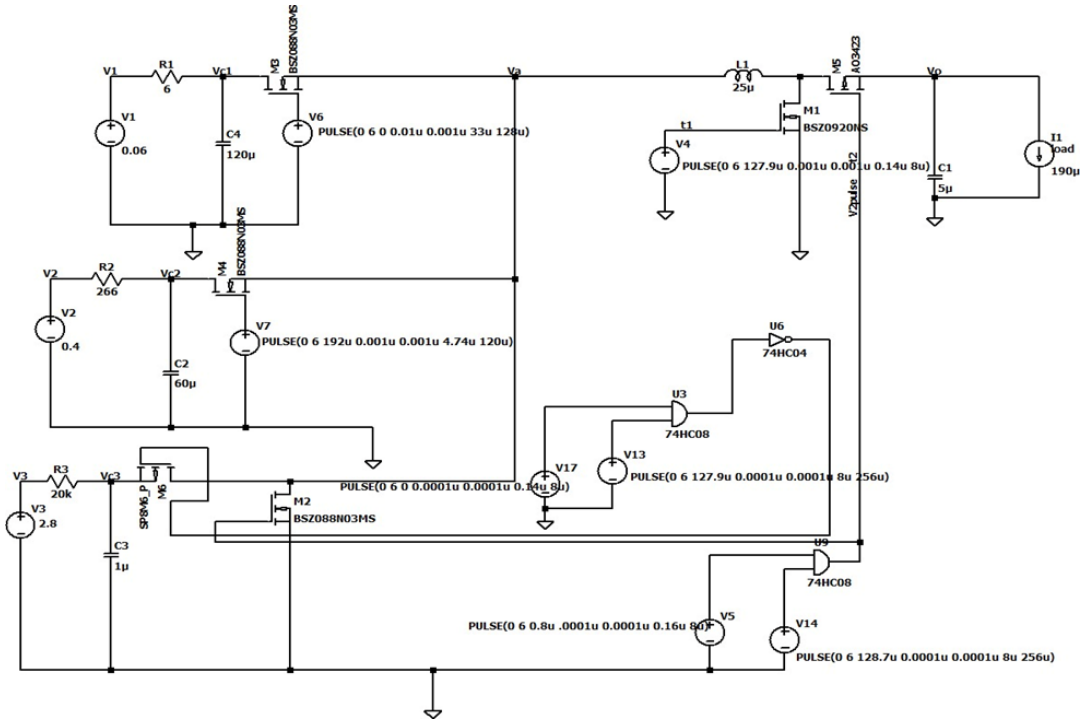

Fig. 4. Schematic for SPICE simulation Framework – Inductor Sharing

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2.4.4. Variants of powerORing, voltage level detection and inductor sharing topologies

The article [31] reiterates catering to multi-level voltage HEH sources with different voltage levels and characteristics and adopts multi-input and multi-output (MIMO) networks using buck-boost converters. Each of the hybrid sources is connected to either a dc-dc or ac-dc converter depending on the type of source and all the outputs are connected to a DC bus, a kind of powerORing based MISO (Multi-input Single Output) configuration. The single DC bus acts as a source for multiple buck-boost converters (each having its own proportional-integral feedback control loop) each one delivering different voltage levels, a kind of SIMO (Single Input and Multi-output) configuration leading to an end-to-end MIMO configuration. Article [32] presents a combiner scheme having dual paths viz. low-power path and high-power path which connects to the load and a battery. Threshold-based comparators and a digital control unit (both together resemble voltage level detection methods) suitably switch the sources to either the low-power path or the high-power path thereby enabling sampling the sources at any time and storing the excess energy in a battery. Article [33] considers PV, TEG and EM (Wind) sources and all are powerORed and further boost converted for charging a supercapacitor (SC), a kind of combined powerORing and inductor sharing. A voltage stabilization circuit provides stable output from SC.

2.4.5. Impedance matching of sources

The article [25] considers resistive matching for PV source, models PZ source with capacitive impedance and resistive and reactive impedance matching for optimal power extraction. The impedance matching is realized with a bidirectional DC-DC converter with MPPT considering PZ impedance is excitation frequency dependent. The article [26] describes energy harvesting from noise and adopts the stochastic resonance (SR) technique and explains the concept of power factor correction to maximize the energy extraction in SR-based energy harvesting by way of allocating/controlling active and reactive components. The article [27] considers modelling electromagnetic and piezo harvesters as lumped reactive transducer elements. The article states that resistive and resistive-reactive impedance-matched loads for EM and PZ sources maximize the harvested power. The article [28] compares the power extracted with modulus impedance and complex conjugate impedance matching for PZ and concludes that due to resonant mode matching, the complex conjugate method generates/extracts 20% more. The article [29] illustrates a resistive-reactive scheme to match the impedance of the PZ device structure for standard energy harvesting (SEH), parallel synchronized switching harvesting on inductor (P-SSHI), and series synchronized switching harvesting on inductor (S-SSHI) interfaces to maximize the power extraction. The article [30] considers the output impedance of PZ as reactive and compares the extraction efficiency for pure resistive load and resistive load with a low pass L matching network to suitably match the reactive component of PZ. Considering TEG and PV exhibit pure resistive impedance, the resistive impedance matching has been carried out in the SPICE modelling and simulation framework illustrated in this paper. Since, PZ exhibits R-C impedance, modulus impedance matching has been adopted.

2.5. HEC circuit topologies – SPICE modelling, simulation and analysis framework

This section presents the SPICE modelling, simulation, and analysis framework on LTSPICE to model and analyze HEC circuit techniques viz. inductor sharing, voltage level detection and powerORing with static analytical models for harvester source transducers-TEG, PV, and PZ (sources), power converters (buck, boost, and buck-boost), MOSFET switches matrix and gate drives timer pulses generators (trigger circuits to schedule the sources) and variable loads. The simulation and analysis have been carried out with a set of parameters, and input/output power levels and arrived at the overall efficiency of the above energy combiner techniques. The SPICE framework needs to support emulating i) Source energy levels and range ii) frequency of source schedules iii) fair combiner algorithm for source schedules iv) voltage references for comparators and v) single or multiple power converters vi) shared inductor vii) modulus impedance matching by switching frequency etc.

2.5.1. Sources and load modelling – inductor sharing, voltage level detection, Power Oring

All sources viz. TEG, PZ and PV are modelled as first-order linear elements with a voltage source and internal series impedance which enables emulating wider source energy level and range. Sources are connected to intermediate storage capacitors and a variable current sink acts as a load for simulation.

2.5.2. Energy combiner with shared inductor

In Inductor sharing method [20], the single power converter acts as an energy combiner with the inductor being shared among multiple sources connected through a switch matrix (one switch per source). In our SPICE framework, nMOS and pMOS switches are used and the power converter has been modelled as an open loop, static converter. ON, OFF and IDLE times of the converter and the number of times the sources are connected to the converter within the assigned timeslot are arrived based on the input voltage level and input impedance of the energy harvesting sources [20]. For evaluating the framework this has been defined as per [20]. Fig 4 presents the schematic for the SPICE simulation. The MOSFET switches and the voltage sources/pulse generators

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enable varying the frequency of scheduling of each source and the combiner algorithm to give a fair chance to all sources. Inductor shared combiner is based on a single DC-DC converter.

Efficiency of the Inductor Shared Combiner Topology - Theoretical Estimates

a) Switching Period: The clock frequency of the combiner (Fclk) is considered as 3.9 KHz, so the clock time-period of the combiner is 256 µsec. Within 256 µsec, the switch matrix (which controls the flow to the inductor) will connect the Thermal source twice, the photovoltaic source eight times and the piezoelectric source once. This time schedule of each source to the combiner (inductor shared dc-dc) is based on source impedance matching (modulus) and voltage level. The dedicated time slot for each source is calculated by multiplying the frequency by the number of times the converter is switched. Fig 5 depicts the time schedule of the sources for various combiner topologies.

As earlier, thermal source will be switching twice within the dedicated, therefore the period can be calculated as,

$$F_{sw,thermal} = 2 * F_{clk} = 7.8kHz \; and \; T_{sw,thermal} = 128\ \mu s \quad (1)$$

Similarly for the photovoltaic and piezoelectric sources, the time schedules are calculated. Therefore, the first 128 µsec of the total period is dedicated to the thermal source, the upcoming 8 µs have been allocated for piezoelectric applications, given that piezoelectric energy harvesters are characterized by their higher effective source impedance. Accordingly, the power conversion/energy combining process for these harvesters necessitates a single switching operation within the designated interval. And, the next 120 µsec is dedicated to photovoltaic.

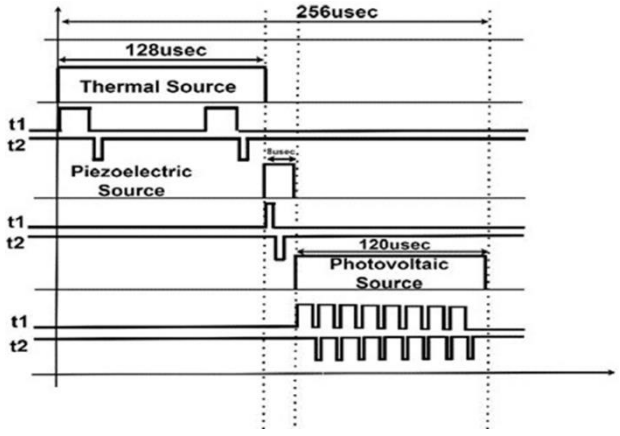

Fig. 5. Schedule of the sources – inductor sharing, voltage level detection, and PowerORing based combiner topologies [20]

b) ON and OFF Period: The ON period is the charging period of the Inductor and the OFF-period is the discharging period of the inductor. The IDLE period is during which inductor current is zero after discharging till the next cycle starts. The ON and OFF state periods for thermal source are calculated as, ON state period

$$t_1 = sqrt[(2 * L)/(F_{sw} * Z_{in})] = 33\ \mu s \quad (2)$$

Here, L is the inductor of the boost converter = 25 µH, Zin is input impedance seen by the boost converter from the Thermal source which is 6 ohms. Next, t_2 or OFF state period for the converter is calculated as,

$$t_2 = \left(\frac{1}{V_o}\right) * \left(sqrt\left[(2 * L * P_{Har})/F_{sw,thermal}\right]\right) = 0.82\ \mu s \quad (3)$$

Here, V_o is the load voltage for the boost converter or the output voltage of the converter which is 1.2V. P_{Har} is the harvested power and is given as,

$$P_{Har} = [V_a^2/Z_{in}] = 150\mu W \quad (4)$$

Va = Harvested voltage or the input voltage to the converter which is half of *Vin* = 30 mV which is due to the converter following the maximum power transfer theorem/voltage divider between the source's internal impedance and converter input impedance. For thermal source Vin = 60 mV. Total time for the thermal source ($T_{total,thermal}$) is the sum of ON, OFF and IDLE time.

$$T_{total,thermal} = 2 * (t_1 + t_2 + T_{IDEAL,thermal\_boost}) \quad (5)$$

From Eqn. (5), Idle time for thermal source is calculated as, $T_{IDEAL,thermal\_boost}$ = 30.18 µs.

c) Efficiency Estimates: The peak-to-peak efficiency when thermal source alone is powering the load is,

$$\%\eta_{peak\ to\ peak\_thermal} = P_{out(avg)}/P_{in(avg)} = (V_o * I_{out(avg)})/(V_{in} * I_{in(avg)}) \quad (6)$$

Here, $\%\ \eta_{peak\ to\ peak\_thermal}$ is the peak-to-peak efficiency or the combiner efficiency with respect to thermal source, Vin is the input voltage from thermal source=60 mV, V_o is the required output voltage=1.2 volt, $I_{in(avg)}$ is the average input current drawn from the source or to the power converter, $I_{out(avg)}$ is the Average output current of the boost converter to the load.

$$I_{in(avg)} = (I_{pk} * (t_1 + t_2))/(2 * T_{sw,thermal\_boost}) \quad (7)$$

Here, I_{pk} = Peak current of the inductor = $((V_a * t_1)/L)$. Peak current is calculated only for t_1 since during t_1 inductor energies and the current through the inductor ramp up and I_{pk} = 39.6 mA. Substituting all the values in Eqn. (7), input average current, $I_{in(avg)}$ = 5.23 mA. I_{pk} for both the input and output remains the same, as a DCM converter is used. In the DCM converter for each cycle, the inductor current starts from zero and comes down to zero at the end of OFF time and remains at zero during IDLE time.

$$I_{out(avg)} = (I_{pk} * t_2)/(2 * T_{sw,thermal\_boost}) \quad (8)$$

Now the average input power can be calculated by,

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$$P_{in(avg)} = V_{in} * I_{in(avg)} = 314\ \mu W \quad (9)$$

Similarly, the output power can be calculated as,

$$P_{out(avg)} = V_o * I_{out(avg)} = 152.4\ \mu W \quad (10)$$

From equation (6),

$$\%\eta_{peak\ to\ peak\_thermal} = 48.5\% \quad (11)$$

Similarly, combiner efficiency with respect to photovoltaic and piezoelectric sources can be calculated. Like the above steps, the efficiencies for the other two sources are calculated. The efficiency estimates for the other two cases are:

$$\%\eta_{peak\ to\ peak\_photovoltaic} = 43.3\% \quad (12)$$

$$\%\eta_{peak\ to\ peak\_piezoelectric} = 23\% \quad (13)$$

The input and output powers for photovoltaic and piezoelectric sources are 2.8 mW, 1.2 mW and 1.702 mW, 0.392 mW respectively. In this analysis, efficiencies are estimated with ideal conditions and switching losses in the converters and losses in discrete components are not considered. Eqns. (11), (12) and (13) are the efficiencies for each of the individual sources. All the inputs are connected in parallel, and the switch matrix connects one at a time to the power converter as per the predefined time schedule within 256 μsec frame and the frame repeats infinitely. Therefore, the total input power will be the summation of the individual input powers and the overall efficiency will be the ratio of output power to the total input power. Overall combiner efficiency is,

$$\%\eta_{overall} = P_{outT}/P_{inT}$$

$$P_{inT} = P_{in1} + P_{in2} + P_{in3} = 1.094\ mW \quad (14)$$

$$P_{outT} = P_{out1} + P_{out2} + P_{out3} = 0.404\ mW \quad (15)$$

$$\%\eta_{overall} = 36.9\% \quad (16)$$

2.5.3. Energy Combiner by Voltage Level Detection and Power ORing techniques

Unlike an inductor-shared combiner, voltage level detection and powerORing need to have an independent dc-dc converter (boost for TEG and PV, buck-boost for PZ) for each source. The input impedance of the dc-dc converter is matched with the harvested source transducer's output impedance by suitably switching the dc-dc converter of each source. The switching frequency depends on the input voltage to the converter and the output voltage to be delievered to the load or to be stored. In voltage level detection and powerORing based combiner, the voltage levels to be combined are already regulated/converted by dc-dc converter.

Fig. 6 and 7 depict block schematics of the simulation framework for voltage level detection and powerORing topologies respectively. The uniformity of the time schedule has been maintained across all combiner topologies, as depicted in Fig. 5. This uniform synchronization ensures a more equitable basis for comparing the various topologies. The MOSFET switches, clock generators, digital control unit and comparators (voltage reference levels, hysteresis etc.) enable varying the frequency of scheduling of each source and the combiner algorithm to give a fair chance to all the sources for voltage level detection-based combiner. In powerORing the source that has the highest harvestable power dominates in the combiner and caters to the load requirements. However, the sources can be scheduled suitably by varying the capacitor values at the output of dc-dc converters. In voltage level detection and powerORing, each source is with a dc-dc converter followed by combiner elements and the following sections present modelling of each sub-block.

Modelling of DC-DC converter

The DC-DC converters are modelled as open loop converters with two assumptions, i) harvested energies from the source are continuous, and the charging and discharging times are fixed. The time schedule of the converters is calculated based on the output impedance of the source and fixed for carrying out the simulations. The converter output voltage for all three sources is considered as 1.8 V and the harvested sources output are provided as inputs to the converters.

Modelling of boost converter for TEG and PV

The converter output of 1.8 V will act as the input voltage for the combiner and the combiner will provide an output voltage of 1.4 V (which is the load requirement). The load current is taken as 120 μA. The output to input voltage ratio is 30 (1.8/0.06 = 30). The input voltage must be boosted up to 30 times to meet the load requirements and a two switches-based DCM mode boost converter is used. Fig. 8(a), shows time pulses for the ON, OFF and IDLE states of the DCM mode boost converter and Fig.8(b) shows the circuit arrangement of the DCM boost converter. Schematically shown in Fig. 8(c), 8(d) and 8(e) present a boost converter in three different states (i.e.: ON, OFF and IDLE state). Switches shown in Fig. 8(b) are modelled by MOSFET. SW1 is modelled by n-MOS transistor and SW2 is modelled by p-MOS. Since the converters are modelled in open-loop, the ON time of the n-MOS switch, the ON time of p-MOS switches, and the OFF-state time of the converter are pre-calculated [19] and pre-defined.

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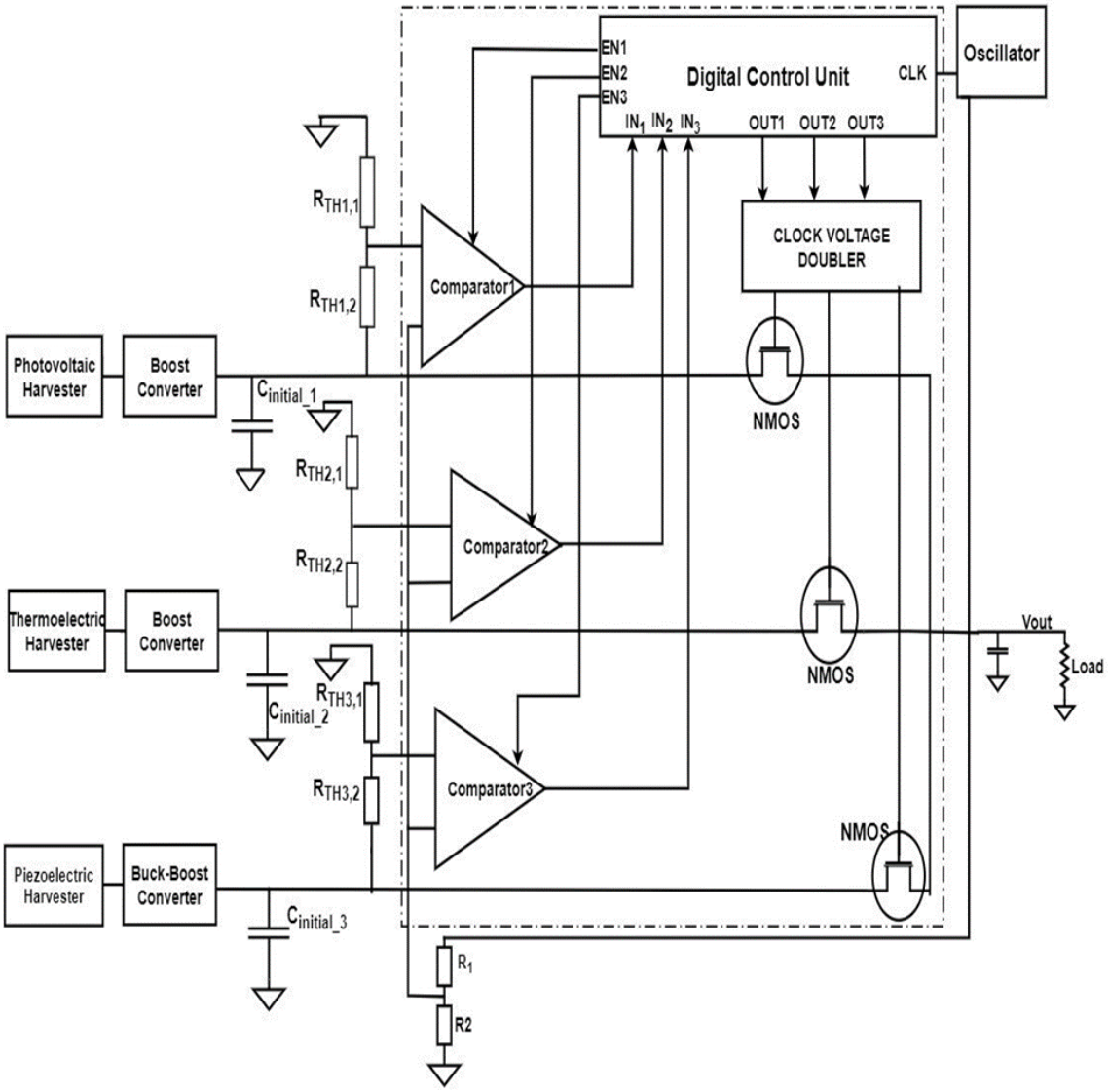

Fig. 6. Block schematic for SPICE simulation framework–voltage level detection [12-13]

Modelling of buck-boost converter for PZ

The piezoelectric source uses four switches buck-boost converter as impedance matching circuit and converter. This buck-boost converter is also modelled in DCM mode. The ON and OFF time of the converter is calculated by using the same equation used for the boost converter.

Overall efficiency for voltage detection method – theoretical estimates and SPICE simulation

a) Switching period: The clock frequency of the combiner (F_{clk}) is considered as 3.9 kHz which gives the Tsw as 256 µsec. Therefore, the first 128 µsec of the total period is dedicated to the thermal source, the next 8 µsec is for the piezoelectric source, and the next 120 µsec is dedicated to the photovoltaic source. Further to derive the efficiency, a photovoltaic source is considered. The same time allocation is considered for Power-ORing method.

b) ON and OFF period: The ON and OFF state periods for photovoltaic source are calculated as, ON state period

$$t_1 = sqrt[(2 * L)/(F_{sw} * Z_{in})] = 4.75\ \mu s$$

Here, L is the inductor of the boost converter = 25 µH, Zin is input impedance seen by the boost converter from the Thermal source which is 266 ohms. Next, t_2 or OFF state period for the converter is calculated as,

$$t_2 = \left(\frac{1}{V_o}\right) * \left(sqrt\left[(2 * L * P_{Har})/F_{sw,photovoltaic}\right]\right) = 0.53\ \mu s$$

t_1 and t_2 are estimated based on resistive and modulus impedance matching requirements of the respective sources. Here, V_o is the load voltage for the boost converter or the output voltage of the converter which is 1.8V. P_{Har} is the harvested power and is given as,

$$P_{Har} = [V_a^2/Z_{in}] = 150\mu W$$

Va = Harvested voltage or the input voltage to the converter which is half of Vin = 0.2 V which is due to the converter following the maximum power transfer theorem. For photovoltaic source Vin = 0.4 V. Total time for the thermal source ($T_{total,photovoltaic}$) is the sum of ON, OFF and IDLE time.

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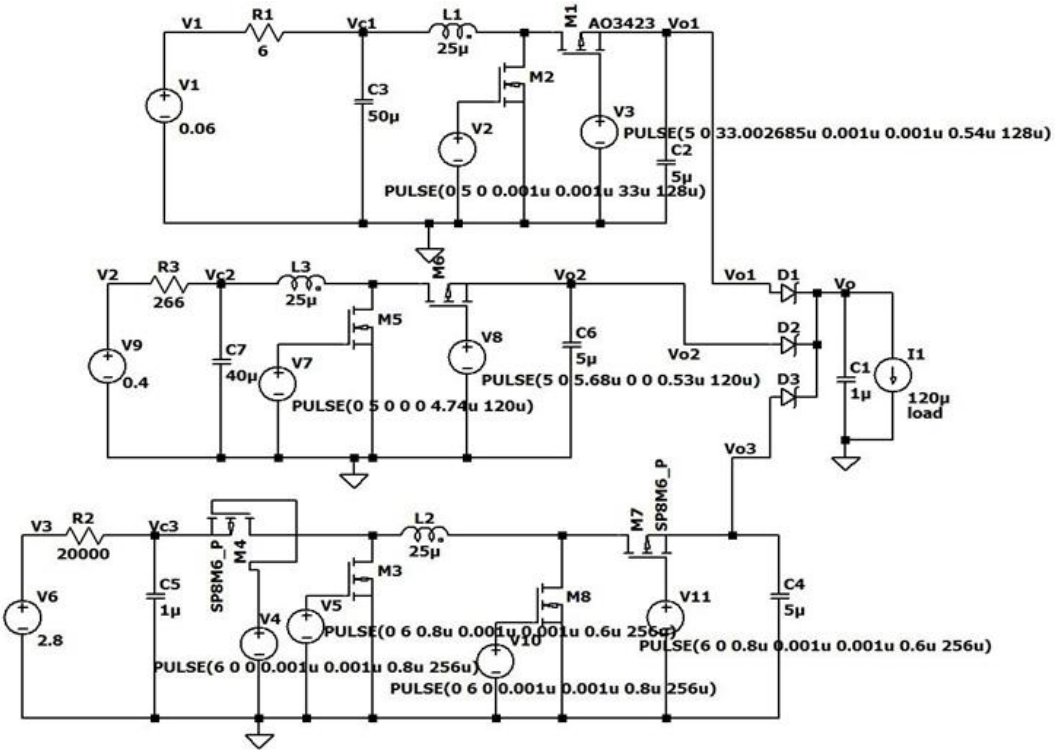

Fig. 7. Block schematic for SPICE simulation framework–powerORing

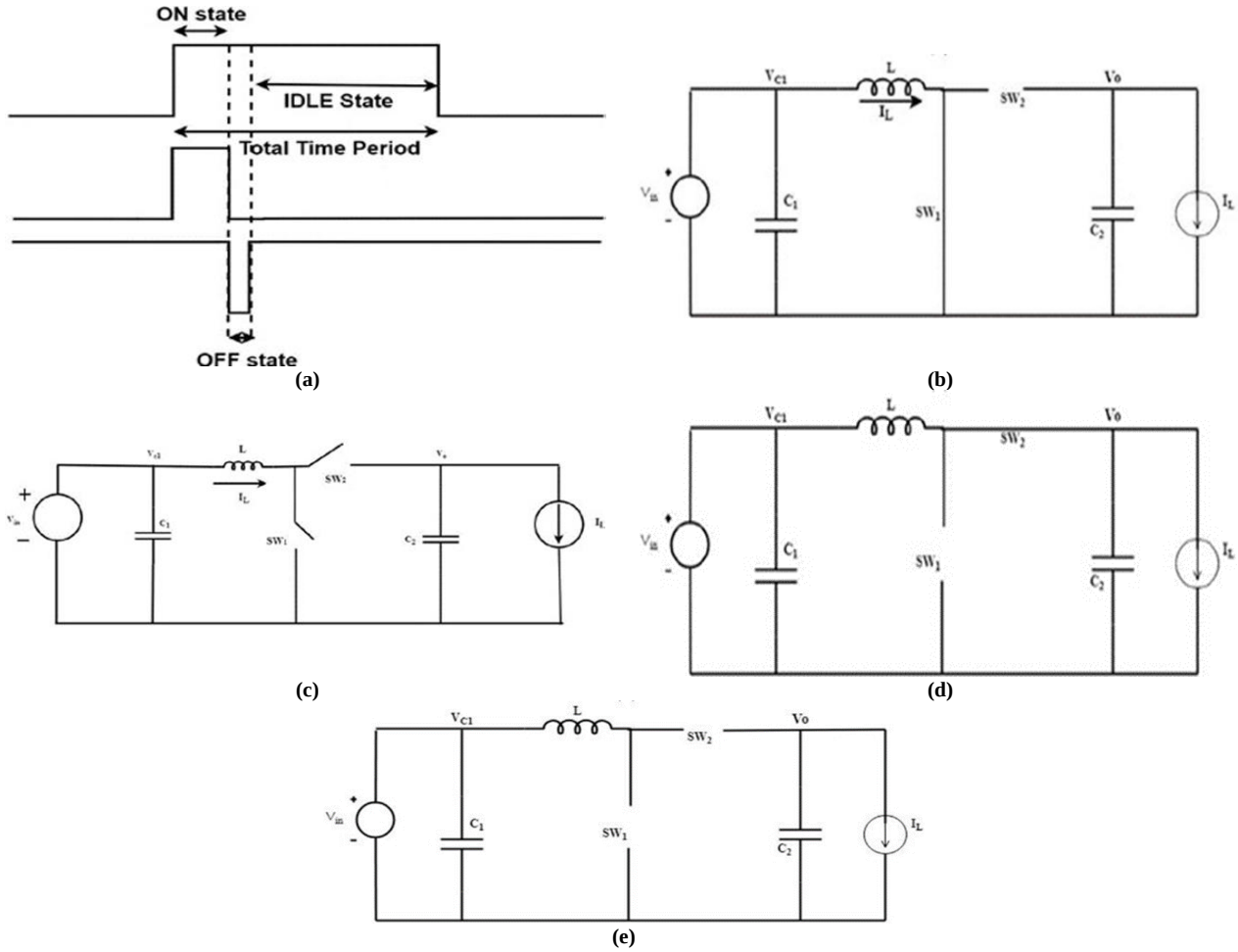

Fig. 8. (a) Time pulses for ON, OFF & IDLE states and total time period of DCM mode dc-dc converter (b) Schematic for DCM boost converter (c) Boost converter in ON (d) Boost converter in OFF (e) Boost converter in IDLE state

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$$T_{total,photovoltaic} = 2 * (t_1 + t_2 + T_{IDEAL,photovoltaic\_boost}) \quad (17)$$

From Equation 17, $T_{IDEAL,photovoltaic\_boost}$ time for photovoltaic source is calculated as, $T_{IDEAL,photovoltaic\_boost}$ = 114.72 µs.

c) Efficiency of combiner estimates for voltage level detection:

For deriving the overall efficiency of the voltage detection energy combiner, the arrangement shown in Fig.9 is used. η1, η2 and η3 shown in the figure are the efficiencies of the first stage. The first stage in the energy combining system is the dc-dc converter stage/impedance matching stage as shown in Fig. 6. Hence, η1, η2 and η3 are the dc-dc converter stage efficiencies. And η is the combiner IC efficiency. Consider η11, η12 and η13 are the peak-to-peak efficiency with respect to individual sources. η11 is the peak-to-peak efficiency with respect to the thermal source (efficiency is calculated from output to the thermal input), η12 is the peak-peak efficiency with respect to the photovoltaic source (efficiency calculated from output to the photovoltaic input) and η13 is the peak-to-peak efficiency with respect to piezoelectric source (efficiency calculated from output to the piezoelectric source).

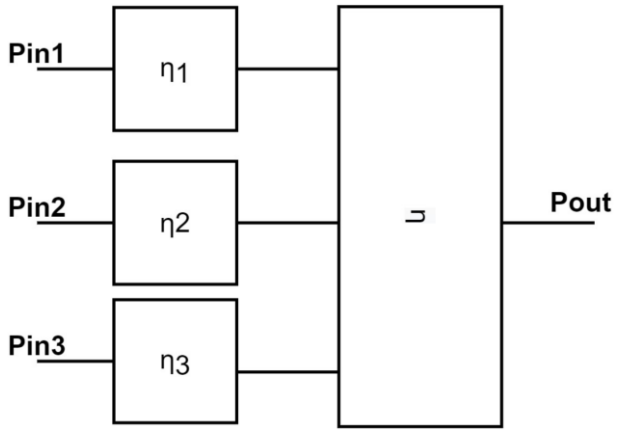

Fig. 9. Overall efficiency calculation – A simplified model

Overall efficiency can be calculated as,

$$\%Overall\ efficiency = [\Sigma^n(\eta 1i * Pini)/\Sigma^n(Pini)] * 100 = [(3 * P_{out})/(P_{in1} + P_{in2} + P_{in3})] * 100 \quad (18)$$

P_{in1}, P_{in2}, P_{in3} are the average input power of thermal, photovoltaic and piezoelectric sources respectively. Here the average input and the output power of photovoltaic are calculated as below,

The average input power can be calculated by,

$$P_{in(avg)} = V_{in} * I_{in(avg)} \quad (19)$$

V_{in} is the input voltage from the photovoltaic source = 0.4 V, $I_{in(avg)}$ is the average input current drawn from the source or to the power converter.

$$I_{in(avg)} = (I_{pk} * (t_1 + t_2))/(2 * T_{Total,photovoltaic}) \quad (20)$$

Here, I_{pk} = Peak current of the inductor = $((V_a * t_1)/L)$. Peak current is calculated only for t_1 since during t_1 inductor energies and the current through the inductor ramp up and I_{pk} = 38 mA. Substituting all the values in Eqn. 20, input average current, $I_{in(avg)}$ = 836 µA. . In the DCM converter for each cycle, the inductor current starts from zero and comes down to zero at the end of OFF time and remains at zero during IDLE time.

$$I_{out(avg)} = (I_{pk} * t_2)/(2 * T_{Total,photovoltaic}) = 84\ \mu A$$

Now the average input power can be calculated by substituting in eqn. (19),

$$P_{in(avg)} = V_{in} * I_{in(avg)} = 334.4\ \mu W$$

Similarly, the output power can be calculated by,

$$P_{out(avg)} = V_o * I_{out(avg)} = 151.2\ \mu W$$

V_o is the required output voltage = 1.8 V, $I_{out(avg)}$ is the average output current of the boost converter to the load. The average input and output powers for thermal and piezoelectric sources are 312 µW, 150 µW and 350 µW, 98.1 µW respectively.

For voltage level detection, the calculated overall efficiency in % is obtained as 51%, by considering output voltage of 1.4V and load current of 120 µA. Similarly, for powerORing method, we can calculate the overall efficiency by the formula derived in equation 18. The output voltage considered in poweORing is 1.2 V and a load current of 120µA. Theoretical estimates in brief for powerORing are presented below.

Overall efficiency of the Power ORing combiner topology – theoretical estimates

Similar to the voltage level detector, the clock frequency of the combiner (F_{clk}) is considered as 3.9 kHz. The first 128 µsec of the total period is dedicated to the thermal source, the next 8 µsec is for the piezoelectric source, and the next 120 µsec is dedicated to the photovoltaic source. All the parameter's formula for finding the overall efficiency of the combiner is the same as that of voltage level detection. However, in the simulation of power ORing the output voltage considered is 1.2 V with a load current of 120 µA, thus the parameters for the photovoltaic energy harvester are as follows:

$$t_1 = 4.75\ \mu sec;\ t_2 = 0.53\ \mu sec;\ I_{pk} = 38mA;$$

$$I_{in(avg)} = 836\ \mu A;\ P_{in(avg)} = V_{in} * I_{in} = 334.4\ \mu W$$

t_1 and t_2 are estimated based on resistive and modulus impedance matching requirements of the respective sources. Similarly, the input power for thermal and piezoelectric sources obtained is 312 µW and 350 µW respectively. Therefore, the overall efficiency of Power ORing is,

$$P_{out(avg)} = 1.2 * 120\mu A = 0.144\ mW$$

$$\%Overall\ efficiency = [(3 * 0.144)/(0.312 + 0.334 + 0.35)] * 100 = 43\%$$

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3. Results and Discussion

The schematic shown in Fig. 4 with energy harvesting sources (as ideal sources) modelled as in Fig. 3 and inductor sharing-based energy combiner topology has been simulated in LTSPICE and the overall efficiency is arrived through simulation. Table 2 shows the calculated and simulated results of the Inductor Shared Combiner Topology.

Table 2. Simulated and calculated parameters for inductor sharing combiner topologies

Parameters	Inductor Sharing	
	Cal.	Sim.
$I_{pk(Thermal)}$ in mA	39.6	36
$I_{pk(Photovoltaic)}$ in mA	38.4	18.24 & 16.2
$I_{pk(Piezoelectric)}$ in mA	8	3.17 & 0.56
$I_{in(avg\_Thermal)}$ in mA	5.23	5.11
$I_{in(avg\_Photovoltaic)}$ in mA	0.9	0.72
$I_{in(avg\_Piezoelectric)}$ in mA	0.15	0.46
$I_{out(avg\_Thermal)}$ in µA	127	150
$I_{out(avg\_Photovoltaic)}$ in µA	130	150
$I_{out(avg\_Piezoelectric)}$ in µA	80	150
$P_{in(avg\_Thermal)}$ in mW	0.314	0.307
$P_{out(avg\_Thermal)}$ in mW	0.152	-
$P_{in(avg\_Photovoltaic)}$ in mW	0.36	0.285
$P_{out(avg\_Photovoltaic)}$ in mW	0.156	-
$P_{in(avg\_Piezoelectric)}$ in mW	0.42	0.128
$P_{out(avg\_Piezoelectric)}$ in mW	0.096	-
$P_{in(avg\_Total)}$ in mW	1.094	0.721
$P_{out(avg\_Total)}$ in mW	0.404	0.233
$\%\eta_{Total}$	36.9	32.4

The calculated and simulation values for voltage level detection and PowerORing are tabulated in Table 3. From Tables 2 and 3, the voltage level detection method stands out with the best efficiency for these three sources. However, efficiency might differ for different scenarios of sources, its variants, schedules etc.

This article presents a detailed evaluation of modelling, simulation, and analysis of diverse topologies for combining energy from multiple sources. These topologies typically undergo comprehensive scrutiny to assess their power consumption and overall energy efficiency. This assessment takes into consideration a range of factors including typical sources of energy harvesting, sources of electrical parameters, input and output power, and more.

This SPICE simulation and analysis framework is highly adaptable. It can be configured with different kinds of sources, energy levels of sources, varying frequency schedules for energy combining, distinct algorithms for combining, single or multiple power converters, as well as different load conditions or requirements. This adaptability empowers the framework to analyse systems through simulations, ultimately yielding an optimal topology for combining energy in specific scenarios. Additionally, it offers the opportunity to explore alternative techniques for combining energy, a prospect that holds promise in overcoming current limitations for designing efficient deployable energy combiners to power self-sustaining autonomous devices. Notably, in our case study with the framework it was observed that the outcomes from calculations and simulations show a strong alignment. Further, for the specific three input sources scenario, the framework enabled the conclusion that voltage level detection along with a DC-DC converter for combining energy demonstrates superior efficiency when compared to other topologies.

Table 3. Hybrid energy combiner topologies- efficiency comparison –theoretical and simulation

Parameters	Voltage Level Detection		PowerORing (Zener Diode)	
	Calc.	Sim.	Calc.	Sim.
$I_{pk(Thermal)}$ in mA	39.6	38.23	39.6	38.23
$I_{pk(Photovoltaic)}$ in mA	38	36	38	36
$I_{pk(Piezoelectric)}$ in mA	45	43	45	43
$I_{in(avg\_Thermal)}$ in mA	5.2	5.16	5.2	5.16
$I_{in(avg\_Photovoltaic)}$ in mA	0.836	0.809	0.836	0.809
$I_{in(avg\_Piezoelectric)}$ in mA	0.125	0.067	0.125	0.067
$I_{out(avg\_Thermal)}$ in µA	83.5	73	83.5	73
$I_{out(avg\_Photovoltaic)}$ in µA	84	112	84	112
$I_{out(avg\_Piezoelectric)}$ in µA	54.5	47	54.5	47
$P_{in(avg\_Thermal)}$ in mW	0.312	0.329	0.312	0.31
$P_{out(avg\_Thermal)}$ in mW	0.15	0.097	0.15	0.131
$P_{in(avg\_Photovoltaic)}$ in mW	0.334	0.317	0.334	0.318
$P_{out(avg\_Photovoltaic)}$ in mW	0.151	0.112	0.151	0.136
$P_{in(avg\_Piezoelectric)}$ in mW	0.35	0.204	0.35	0.194
$P_{out(avg\_Piezoelectric)}$ in mW	0.098	0.0574	0.098	0.082
$P_{in(avg\_Total)}$ in mW	0.996	0.850	0.996	0.876
$P_{out(avg\_Total)}$ in mW	0.168	0.501	0.144	0.395
$\%\eta_{overall}$	51	58.9	43	45

Presently, the parameters for SPICE models and the simulation framework are predetermined and provided as inputs. However, there's potential for these to be dynamically estimated based on a set of customizable input parameters. These parameters can encompass the electrical traits of energy sources, the desired final output voltage, and the preferred scheme for matching impedance. Furthermore, there's a possibility for the framework to incorporate a customizable electrical model for sources and handling the impedance matching of mechanical-to-electrical variables of the sources.

4. Conclusion

In order to investigate if this SPICE framework can effectively simulate various combiner topologies that have been published, a comparison and analysis is detailed in Table 4. Certain articles ([5], [7], [23], [31], [33], [35], [37]) that deal with commercial off-the-shelf (COTS) ICs or systems, systems design, reviews, or studies have been left

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out from this comparison. Also, references [25] to [30] mainly focus on matching sources and power converters in terms of impedance, and don't emphasize the ways to combine energy, which is why they aren't part of Table 4. However, the matching methods adopted in the references are summarized in Table 4.

The last column indicates whether the SPICE framework presented in this article can model the combiner topologies illustrated in the references cited in the first column. The input-output refers to single/multiple inputs/outputs. It is evident that our framework can handle most of the references quite well except the MPPT schemes, start-up circuits and impedance matching schemes other than switching frequency-based matching. Additionally, our framework does not include ways to combine energy using LDOs and charge pumps.

Table 4. Our SPICE Simulation Framework Vs Energy Harvester Combiner Topologies in References: Modelling Viability Analysis

Ref. No.	Energy Harvester Sources	Energy Combiner		MPPT	Start-up Circuit	Sources Time Schedule Controller	Source to Converter - Impedance Matching	Can our SPICE Framework model this?
		Switching Technique	Input-Output					
[6]	TEG, PV	Inductor Sharing	MISO	Voltage Reference based	No	Yes	Switching Frequency	Yes, Except MPPT.
[8]	TEG, PZ, EM	Output power ORing	MISO	Switching Frequency	No	Yes	Switching Frequency	Yes
[10]	TEG, PZ	Output powerORing	MISO	Switching Frequency	No	Yes	Switching Frequency	Yes
[11]	TEG, PV, PZ, MI	LDO, Output powerORing	MISO	Switching Frequency	No	Yes	Switching Frequency	No. Our does support LDO-based converters
[12] [13] [14]	Generic –All inputs are DC	Voltage Level Detection	MISO	Not Applicable – Only energy combiner	Not Applicable	Yes	Not Applicable – Only Energy Combiner	Yes. The Energy Combiner can be modelled
[15]	MFCs	Time Multiplexed	MISO	No	Yes. Charge pump	Yes. Counter-output-based sequencing	Switching Frequency	Yes. Except the Charge pump.
[16]	TEG, PZ	Output power ORing and Time MUXed	MISO	No	No	Time MUXed to load	No	Yes.
[17]	EM, PZ	Inductor Sharing	MISO	Yes. Synchronous Extractor	Yes	Yes	Synchronous Extractor	Yes. Except for MPPT, start-up and impedance matching
[19]	EM, PZ	Inductor Sharing	MISO	OCV based	No	Yes	Switching Frequency	Yes. Except MPPT.
[20]	TEG,PZ, PV	Inductor sharing	MISO	Hill climbing.	Yes	Yes	Switching Frequency	Yes. Except MPPT and start-up
[22]	TEG, PV, RF	Inductor Sharing	MISO	Synchronous Extractor, Fractional OCV	Yes	Yes	Synchronous Extractor	Yes. Except, MPPT, start-up and impedance matching
[24]	PZ, EM – Both sources are coupled	Inductor Sharing	MISO	Synchronous Extractor	No	Yes.	Synchronous Extractor	No. Our model does not support coupled sources.
[32]	Generic –All inputs are DC	Voltage Level Detection	MISO	Not Applicable – Only energy combiner	Not Applicable– Only Energy Combiner	Yes	Not Applicable – Only Energy Combiner	Yes. The Energy Combiner can be modelled
[34]	TEG, MFC, PV	Output PowerORing – One power converter (inductor) per source	MISO	No	Yes. Charge pump	Yes	Switching Frequency	Yes and MFC as a dc source. Except Start- up circuit.
[36]	PV, PZ, RF	Inductor Sharing	MISO	OCV based.	Yes	Yes	Switching Frequency	Yes and RF input is equivalent to dc source. Except for MPPT and start-up circuit
[38]	TEG, PV	Inductor Sharing	MISO	Adaptive Pulse Counting Control	No	Yes	Adaptive Pulse Counting Control	Yes. Except for MPPT and adaptive Impedance matching
[39]	PV, PZ	Charge Pump / Switched Capacitor	MISO	Hill Climbing and switched cap. Conversion ratio controlled	No	Switched Cap. Sequencing of the two sources.	Switched Cap. Conversion ratio based.	No. Our SPICE model does not support switched capacitor topology
[40]	PV, MFC	Inductor Sharing	MISO	No	Charge Pump	Yes	Switching Frequency	Yes. Except for the Start-up circuit
This Work	TEG, PV, PZ	Output, Power, ORing – One inductor per source, Inductor Sharing, Voltage Level Detection	MISO	Switching Frequency	No	Yes	Switching Frequency	Implemented

Note: *MPPT – Maximum Power Point Tracking; TEG – Thermoelectric Generator; MFC – Microbial Fuel Cell; PZ – Piezoelectric; TENG – Triboelectric Nano-generators; RF –Radio-frequency; EM – Electromagnetic; MI – Inductive Power Link; MISO – Multi-input Single Output; MIMO – Multi-input Multi-output; OCV – Open Circuit Voltage; FOCV – Fractional Open Circuit Voltage*

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Authorship contribution statement for Contributor Roles Taxonomy

David Selvakumar: Conceptualization, Original Draft, Writing, Technical Reviews, Investigation, Analysis. **Mervin J:** Methodology, Design, Writing, Reviews. **Anurupa Ghosh:** Circuit Design, Simulation, Testing, Evaluation, Writing. **Arnab Deb:** Design Review, Simulation, Testing, Evaluation.

Conflict of interest

The author(s) declares that he has no conflict of interest.

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