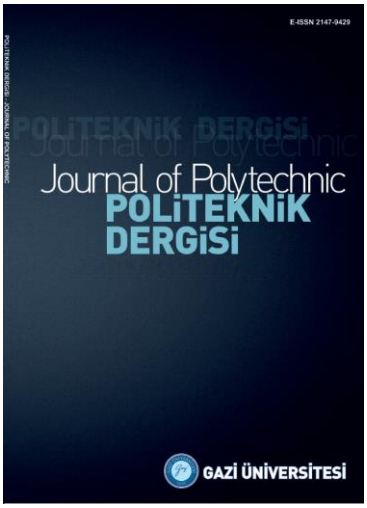

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DC/DC boost converter topologies and experimental comparison in electric vehicle to grid applications

Elektrikli araçtan şebekeye uygulamalarındaki DA/DA yükseltici dönüştürücü topolojileri ve deneysel karşılaştırması

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DC/DC Boost Converter Topologies and Experimental Comparison in Electric Vehicle to Grid Applications

Highlights

- *dc/dc boost converter circuits in wireless charging systems have been analyzed.*
- *High efficiency is achieved with the interleaved boost converter circuit.*
- *Low output current ripple has been demonstrated in experimental studies.*

Graphical Abstract

Synchronous boost converter (SBC) and interleaved synchronous boost converter (ISBC) topologies were examined in this study. Performance comparison was made by analyzing each circuit topology with the experimental results.

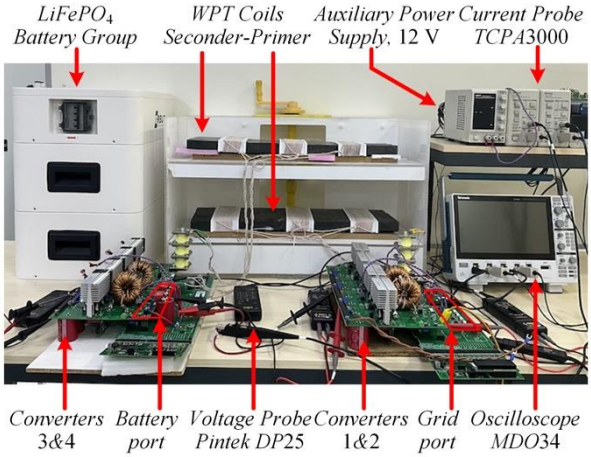

Figure: Photograph of the experimental setup

Aim

To identify high efficiency and low volume dc/dc boost topology to extend the range of the electric vehicles (EV).

Design & Methodology

Synchronous boost converter and interleaved synchronous boost converter circuits were designed. The battery group was discharged with a closed-loop control algorithm. Experimental efficiency results of the SBC and ISBC circuits under different duty cycles are given.

Originality

Comparison experiments of different dc/dc boost converter circuits have been conducted. The selection of high-efficiency circuit topology for EVs is presented with evidence.

Findings

The performance analysis of the SBC and ISBC circuits showed that the ISBC circuit operates with low current ripple and high efficiency.

Conclusion

This study shares the performance analysis of the dc/dc boost converter topologies used in electric vehicles at different duty cycles. Battery charge/discharge circuits in the EVs must be low volume and high efficiency. This study gives experimental results of the synchronous boost and interleaved synchronous boost converter topologies in the literature. Experimental test results prove that the ISBC circuit is the most efficient topology. It has been observed that the ISBC circuit topology operates at 1249 W output power, 0.91 A output current ripple, and 99.09% efficiency. These results show that using ISBC circuit topology in high-power charge/discharge applications for EVs is advantageous.

Declaration of Ethical Standards

This article's author(s) declare that the materials and methods used in this study do not require ethical committee permission and/or legal-special permission.

DC/DC Boost Converter Topologies and Experimental Comparison in Electric Vehicle to Grid Applications

Araştırma Makalesi / Research Article

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ABSTRACT

In applications that transfer energy from the electric vehicle (EV) to the grid, the direct current (dc)/dc boost converter circuits on the vehicle must be light, low volume, and high efficiency. To achieve this advantage, the inductor sizes used in non-isolated dc/dc converter circuits must be reduced. Synchronous and interleaved synchronous topology structures are used in dc/dc boost converter circuits. This study conducted experimental performance analyses of these two dc/dc boost circuits in a system with a battery group and a wireless EV charging structure. The study presents that in the interleaved synchronous dc/dc boost topology at the same power values, inductor currents and output voltage/current ripple decrease, and efficiency increases. The performance characteristics of the two circuit topologies under different operating conditions have been experimentally proven. It has been shown that using interleaved synchronous dc/dc boost converter topology is advantageous in EVs' high charge/discharge applications.

Keywords: Synchronous boost converter, interleaved synchronous boost converter, electric vehicles, wireless power transfer.

Elektrikli Araçtan Şebekeye Uygulamalarındaki DA/DA Yükseltici Dönüştürücü Topolojileri ve Deneysel Karşılaştırması

ÖZ

Elektrikli araçtan (EA) şebekeye enerji aktaran uygulamalarda araç üzerinde yer alan doğru akım (da)/da yükseltici dönüştürücü devrelerinin hafif, düşük hacimli ve yüksek verime sahip olması gerekmektedir. Bu avantajı saplamak için izolesiz da/da dönüştürücü devrelerinde kullanılan bobin boyutlarının düşürülmesi gerekmektedir. da/da yükseltici dönüştürücü devrelerinde senkron ve serpiştirilmiş senkron topoloji yapıları kullanılmaktadır. Bu çalışmada, deneysel olarak bu iki da/da yükseltici devresinin, batarya gurubu ve kablosuz EA şarj yapısı bulunan bir sistemdeki performans analizleri gerçekleştirilmiştir. Çalışmada aynı güç değerlerinde serpiştirilmiş senkron da/da yükseltici topolojisinde bobin akımlarının ve çıkış gerilim/akım dalgalanmalarının azaldığı, verimin artış gösterdiği sunulmuştur. Farklı çalışma şartlarında iki devre topolojisinin performans karakteristikleri deneysel olarak kanıtlanmıştır. EA araçlarda yüksek şarj/deşarj uygulamalarında serpiştirilmiş senkron da/da yükseltici dönüştürücü topolojisinin kullanılmasının avantajlı olduğu gösterilmiştir.

Anahtar Kelimeler: Senkron yükseltici dönüştürücü, katlı senkron yükseltici dönüştürücü, elektrikli araçlar, kablosuz güç transferi

1. INTRODUCTION

Vehicle-to-Grid (V2G) [1] and Wireless Power Transfer (WPT) [2] technologies represent a tremendous milestone with the increasing popularity of electric vehicles (EVs) and the rapid development of smart grid technologies. V2G is an application aimed at integrating electric vehicles into the grid to optimize energy resources. EV's can be used as distrubuted energy sources in to the grid. As a result, vehicles not only transfer energy stored [3] in the battery back to the grid but also contribute to the sustainability of the grid [4]. This contributes to meeting personal needs while ensuring energy continuity in the grid.

WPT is a charging technology [5] used to connect electric vehicles to the grid. This system, providing wireless energy transfer, supports the seamless integration of EVs into the grid [3] by making the charging or discharging process more user-friendly and flexible. Wireless charging can achieve charging [6] using a charging coil placed under the electric vehicle. In this way, drivers can automatically charge when they park their vehicles or move within a certain area. This flexibility eliminates the need for users to be at a specific

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location or stop to charge their vehicles, making daily use of electric vehicles more practical. V2G and WPT technologies [7] enable electric vehicles to become active players in energy systems beyond being just a means of transportation, contributing to the establishment of a sustainable energy system.

During the transfer of battery energy to the load, there is a need for power converter to raise or lower the direct current (dc) obtained from a battery to a higher or lower voltage. These converters ensure controlled discharge of the battery by regulating the current and voltage obtained from the battery, thus protecting the battery. Among these converters [8], synchronous boost converters (SBC) [9] are a specific type of dc/dc converter topology [10] used in implementations where the battery terminal voltage is lower than the load voltage. One of these circuits, the SBC [11], provides higher efficiency by using MOSFET or IGBT instead of diodes found in traditional boost converters. This reduces power losses due to the forward voltage of the diode. As a result, there is less power loss during energy transfer.

In high-power applications, interleaved synchronous boost converters (ISBC) [12] are an good decision with some benefits over SBC [13]. In ISBC [14], the input current is divided by the number of phases[15]. This reduces current stress on semiconductor switch, inductors and capacitors. Low current ripple can contribute to increased efficiency and reduced electromagnetic interference. Additionally, the decrease in current ripple and distribution of power among phases contribute to reducing conduction and switching losses. Another advantage is that ISBC allows for an increase in power processing capacity. Each phase operates at a power value obtained by dividing the total power by the number of phases. In ISBC designs, each phase handles a portion of the total power, reducing thermal stress [16] on individual components. Distributing power among multiple phases allows for better heat dissipation. ISBC, compared to SBC , allows for the use of smaller input and output capacitors [17] while managing the same power. This can be advantageous in applications where lifetime constraints are critical factors. Thanks to the many advantages of ISBC, the overall efficiency of the interleaved synchronous boost converter higher than that of a SBC [18].

This article covers the following topics. Section II explains the synchronous boost converter, interleaved synchronous boost converter circuit topologies, and output current ripple analy. Section III analyzes experimental study results and mentions the experimental test setup. In this section, SBC and ISBC output current ripple analysis and efficiency comparisons are made. Section IV contains the conclusion.

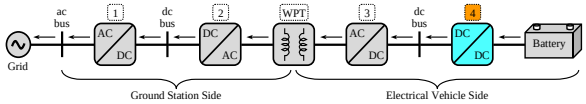


Figure 1. Single-line topology of the EV wireless power transfer system

2. dc/dc BOOST CONVERTER TOPOLOGIES

In power electronics, asynchronous boost converter (ABC), synchronous boost converter (SBC), and interleaved synchronous boost converter (ISBC) topologies are used to increase the input/output voltage gain [9]. ABC and SBC voltage and current characteristics are the same [19]. This study examines and explains SBC and ISBC topologies under the following headings.

2.1. Synchronous Boost Converter (SBC)

SBC circuit topology includes a phase leg consisting of two semiconductor switches. This converter topology takes its name from the principle of switching the switches synchronously with a phase shift of 180°. Schematic and operating modes of the SBC are given in Fig. 2.

The output voltage v_{out} gain of the SBC circuit is related to the duty cycle D ratio and can be expressed as follows.

$$v_{out} = \frac{v_{bat}}{(1-D)} \tag{1}$$

The inductance current ripple of the SBC circuit is expressed by Eq. (2).

$$\Delta i_{L\_SBC} = \frac{v_{bat}\, D}{f_s\, L_{boost}} \tag{2}$$

where, v_{bat} is the battery group voltage, f_s is the switching frequency, L_{boost} is the inductance value. The L_{boost} value in the SBC circuit can be written as follows.

$$L_{boost} = \frac{v_{bat}\, D}{f_s\, \Delta i_{L\_SBC}} \tag{3}$$

The output voltage ripple at the SBC circuit output is related to the output current and is expressed in Eq. (4).

$$\Delta v_{out\_SBC} = \frac{i_{out}\, D}{f_s\, C_{out}} \tag{4}$$

where, i_{out} is the circuit's output current, C_{out} is the output capacitance of the SBC circuit. The output capacitance C_{out} value is given as follows.

$$C_{out} = \frac{v_{out}\, D}{\Delta v_{out\_SBC}\, R_{out}\, f_s} \tag{5}$$

where; R_{out} is the output resistance of the SBC circuit. In this study, Δi_{L_SBC} is designed to be a maximum of 20%, Δv_{L_SBC} is designed to be a maximum of 0.15%.

In the SBC topology, switching elements and diodes operate under high current stresses at high powers. In high-power applications, since the losses of the circuit elements are high, a high-volume design emerges, and dc-to-dc efficiency decreases. Therefore, increasing the number of coils and switching elements in the circuit will improve the system's performance.

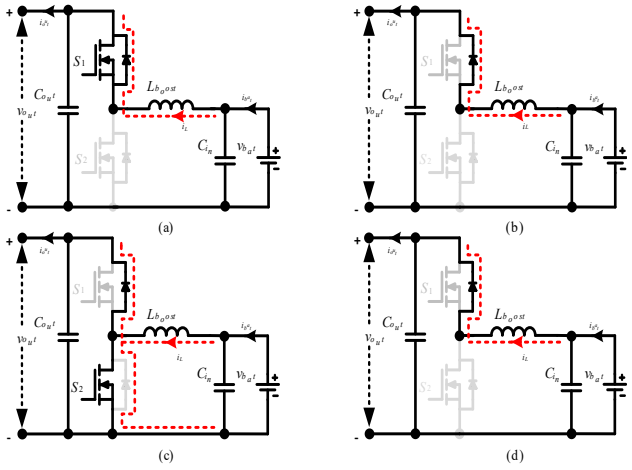


Figure 2. Schematic and operation modes of the asynchronous boost converter: (a) S_1 is on, and S_2 is off, (b) the first case where inductors are discharged with diode, (c) S_2 is on, and S_1 is off, (d) the second case where inductors are discharged with diode

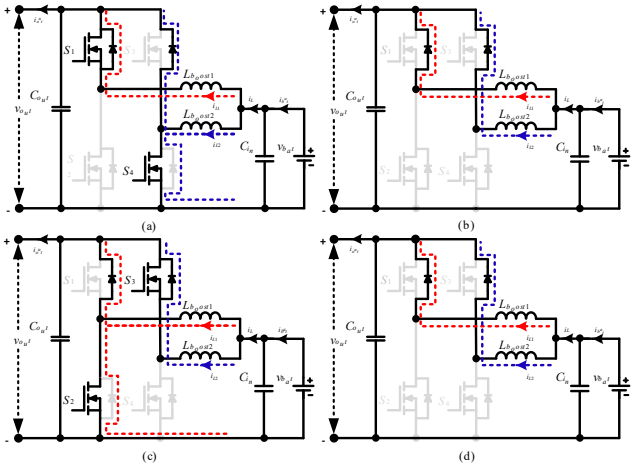


Figure 3. Schematic and operation modes of the interleaved synchronous boost converter: (a) S_1 and S_4 are on, S_2 and S_3 are off, (b) the first case where inductors are discharged with diodes, (c) S_1 and S_4 are off, and S_2 and S_3 are on, (b) the second case where inductances are discharged with diodes

2.2. Interleaved Synchronous Boost Converter (ISBC)

ISBC circuit topologies consist of two or more layers. In this circuit topology, the input current is shared in proportion to the number of inductors in the circuit $i_{bat}=i_{L1}+i_{L2}$. Thus, while the inductor volume in the circuit decreases, the circuit elements operate in a low current stress. This study uses a two-layer ISBC circuit topology, and the circuit schematic and operating modes are given in Fig. 3. The phase shift of 180° gate signals is applied to the $S_1 - S_4$, $S_2 - S_3$ switches in the ISBC circuit.

When examining the gate signals and inductance currents in Fig. 4, it is observed that during the 0-t_1 interval, S_2 is in the off case, causing a decrease in i_{L1}, while S_4 is in the on case, resulting in a linear increase in i_{L2} (Fig. 3 (a)). In the t_1-t_2 interval, both S_2 and S_4 switches are off, and as the diodes of S_1 and S_3 switches allow i_{L1} to continue decreasing, the i_{L2} current transitions from an increase to a decrease (Fig. 3 (b)). During the t_2-t_3 interval (Fig. 3 (c)), as S_1 transitions to the conducting case, i_{L1} starts to linearly increase, and since S_4 remains in the off case, i_{L2} continues to decrease (Fig. 3 (c)). In the t_3-T interval, with both S_2 and S4 switches off, and the diodes of S_1 and S_3 switches allowing i_{L2} to continue decreasing, i_{L1} transitions from an increase to a decrease (Fig. 3 (c)).

The inductor current ripple Δi_{L_ISBC} value of the ISBC circuit can be written as follows.

$$\Delta i_{L\_ISBC}=\frac{v_{bat}\,(1-q_s)\,q_s\,\tau}{f_s\,L_{boost}\,(1-D)} \qquad (6)$$

where, q_s is the input current occupancy-void ratio, τ is the fluctuation period of the input current. The output voltage ripple Δv_{L_ISBC} value of the ISBC circuit is expressed in Eq. (7).

$$\Delta v_{out\_ISBC}=\frac{v_{out}\,q_s\,(1-q_s)}{N^2\,f_s\,R_{out}\,C_{out}\,(1-D)} \qquad (7)$$

where, N is the number of layers of the ISBC circuit. For the ISBC circuit, τ and q_s variables are obtained using Eq. (8) and Eq. (9).

$$q_s=\frac{\tau_{on}}{\tau} \qquad (8)$$

$$\tau=\frac{T_s}{N} \qquad (9)$$

where, T_s is the switching period, and τ_{on} is the input current occupancy rate.

Fig. 4 shows the switching signals, the normalized waveforms of the inductor output current, and current ripple changes of the SBC and ISBC circuits for D=0.4. The normalized current graphs show that the output current ripple value of the ISBC circuit is less than the SBC circuit.

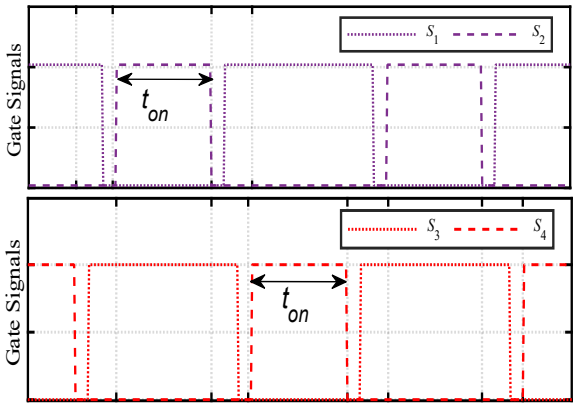


Figure 4. Switching signals and normalized current waveforms of the ISBC

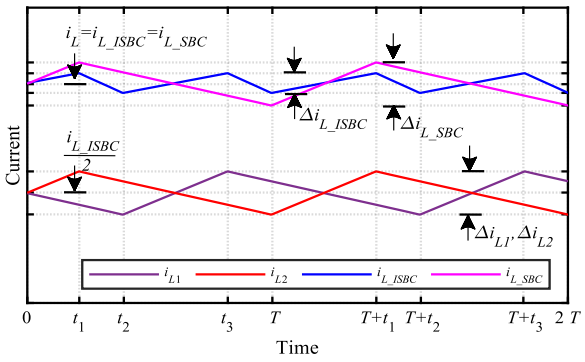


Figure 4. (cont.) Switching signals and normalized current waveforms of the ISBC

Table 1. Comparison of the advantages and disadvantages of the SBC and ISBC topologies

Descriptions	SBC	ISBC
Number of the switch	2	4
Number of the inductance	1	2
Current stress	High	Low
dc-to-dc efficiency	Low	High
Size of the design	High	Low
Power range	Low	High
Input current ripple	High	Low
Output voltage ripple	High	Low
Switching losses	High	Low

The ISBC circuit has advantages over the SBC circuit in terms of high dc-to-dc efficiency, high power range, low input voltage/current ripple, and low switching losses. Table 1 includes compares the SBC and ISBC topologies. The ISBC circuit is suitable for EVs regarding high efficiency and thermal performance.

2.3. Output Current Ripple Analysis

The interleaved dc/dc boost circuit coefficients are proportional to the operating period, $2\pi/N$. The normalized current waveforms show that the input current ripple decreases depending on the circuit layer. Fig. 5 shows the normalized input current ripple graph depending on the D ratio of the SBC and ISBC circuit topology. Theoretically, at a rate of D 0.5, the current ripple value is 0. In the ISBC circuit topology, the input current is shared in proportion to the number of layers. Since the energy stored in the inductors is shared equally, the inductor volumes used in the circuit are reduced.

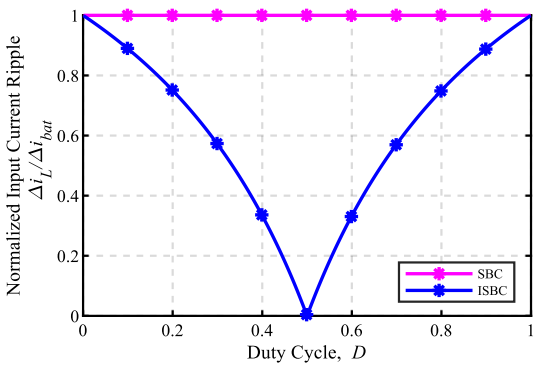


Figure 5. Normalized input current ripple graphs of the synchronous boost and the two-layer ISBC

Fig. 6 shows the graph of the normalized output capacitor current of the SBC and ISBC circuit topologies. In the two-layer circuit, the peak output current value of the capacitor is half. If the output capacitor current value decreases, the capacitor power loss decreases. Meanwhile, the voltage stress on the output capacitor is reduced. Reducing the stresses on the elements in the ISBC circuit increases the circuit's performance and reliability.

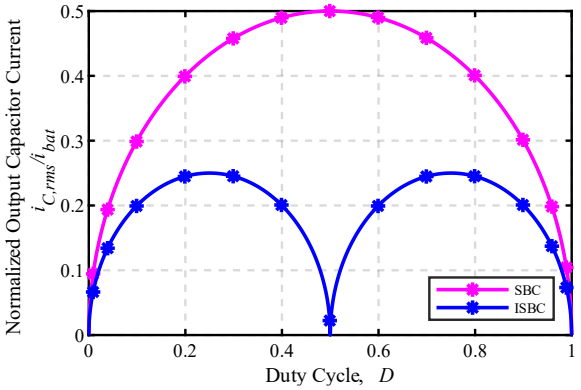


Figure 6. Normalized output capacitor current ripple graphs of the synchronous boost and the two-layer ISBC

2.4. Inductor Design

In this study, the authors produced the inductor used in the dc/dc boost converter circuits and its photograph is given in Fig. 7. From the equations in the circuit topologies, the required value for the inductor was calculated as 500 µH. The core number 0078617A7 of the Magnetics brand was chosen for the inductor prototype. The manufacturer gives this core cross-sectional area an A_L value of 189±8% nH/T^2. The A_L value of the core material varies depending on the current passing through the conductor. According to the technical report provided by the manufacturer, there is a decreasing curve of the A_L value. The maximum discharge current value of the battery group in this study is 25 A. When 25 A passes through the inductor, the A_L value becomes 125 nH/T^2 according to the dc bias performance curve. In Eq. (10), the inductance value formula depends on the core cross-sectional area.

$$L = A_L \, T^2 \, 10^{-9} \qquad (10)$$

According to Eq. (10), for the design value L_{boost} 500 µH, the number of windings must be 52 turns.

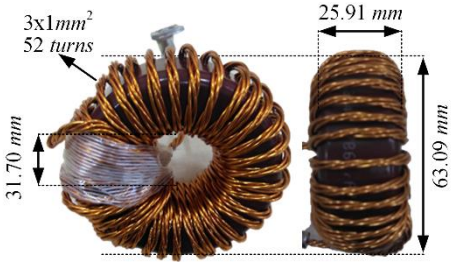


Figure 7. Photograph of the prototyped inductor

Table 2. Parameters of the dc/dc boost converter circuits

Descriptions	Parameters	Value
Battery voltage range	v_{bat}	160 – 195 V
Maximum battery current	i_{bat_max}	25 A
Nominal power	P_{nom}	3.5 kW
Maximum battery current	i_{bat_max}	25 A
Nominal power	P_{nom}	3.5 kW
Input capacitance	C_{in}	560 µF 470 nF
Input capacitance resistance	R_{C_in}	54 mΩ (560 µF) 4.49 mΩ (470 nF)
Output capacitance	C_{out}	560 µF × 2 || 4 470 nF || 4
Output capacitance resistance	R_{C_out}	54 mΩ (560 µF) 4.49 mΩ (470 nF)
Inductance current ripple	Δi_{out}	20 %
Capacitance voltage ripple	Δv_{out}	0.15 %
Inductance	L_{boost}	500 µH
Inductance resistance	R_{L_boost}	40 mΩ
Core cross-sectional area	A_L	189±8% nH/T^2
Number of turns	T	52

In the SBC circuit, high currents pass through the inductor at high power. In this case, the core cross-sectional area A_L value takes lower values. As a result, the number of conductor windings in the inductor increases, and the losses in the inductor increase. In the ISBC circuit topology, the number of inductor windings decreases since the current value passing through the inductor is lower. Thus, a lower volume inductor is used, achieving high efficiency. The parameters of the circuits and the prototyped inductor are given in Table 2.

3. EXPERIMENTAL STUDY AND RESULTS

In the study, a prototype was produced to test the SBC and ISBC circuits. Fig. 8 shows the experimental setup of the dc/dc boost converter circuits, measurement/control card, and EV battery group. The authors manufactured the inductors of the SBC and ISBC circuits, as mentioned in the inductor design section. Wurth brand 470 nF film capacitors and 560 µF aluminum electrolytic capacitors were preferred as the circuit input and output filter capacitors. In this study, the use of a 560 µF electrolytic capacitor with 470 nF film capacitors aims to achieve performance across a wide frequency range. Electrolytic capacitors are generally more effective at lower frequencies with their larger capacitance, while film capacitors can exhibit better performance at higher frequencies. This combination seeks to optimize performance at both low and high frequencies, thereby enhancing the overall circuit performance.

A 200 V 24 Ah rated lithium iron phosphate ($LiFePO_4$) EV battery was connected to the dc/dc boost circuit input. There is a 650 V, 49 A, C3M0045065K SIC MOSFET of the Wolfspeed brand in the dc/dc boost converter power stage. Infineon Technologies 1ED020I12B2XUMA1 integrated circuit was used as the gate driver. Semiconductor switches were controlled by a phase-shifting method with STMicroelectronics' STM32H750 microcontroller. SIC MOSFETs are switched by the control card with a switching frequency of 50 kHz. The dead time between the semiconductor switches on the phase leg in the dc/dc boost circuits is 200 ns. The SIC MOSFET datasheet indicates a turn-on delay time of 9 ns, rise time of 12 ns, turn-off delay time of 18ns, and fall time of 6 ns. Since the sum of these time values is less than 200 ns, the chosen dead time value is considered reliable for the switching process. In experimental studies, circuit voltages and currents were recorded with a Tektronix brand MDO34 (350HHz) model oscilloscope.

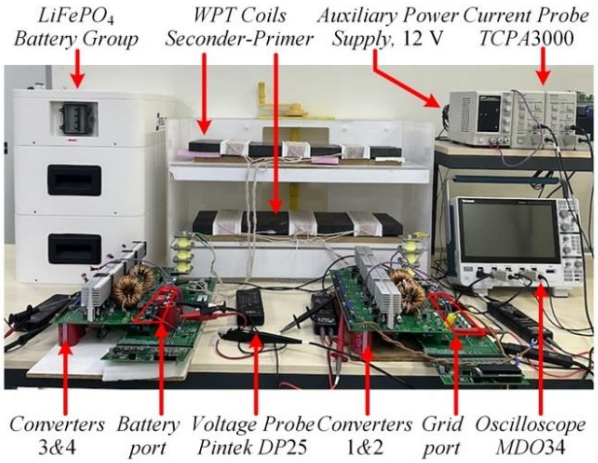
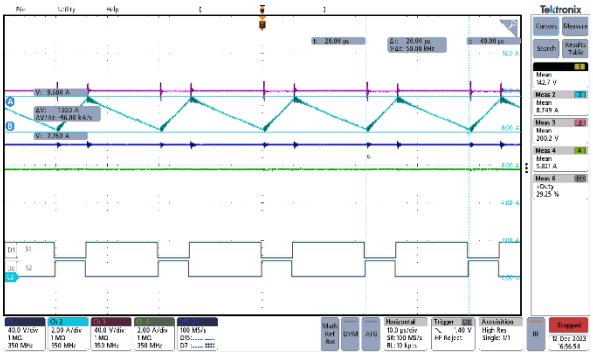


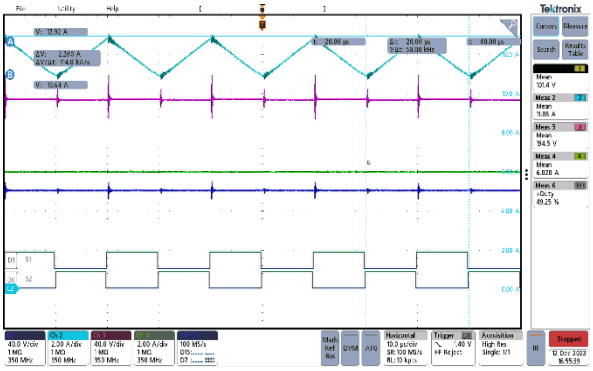
Figure 8. Photograph of the experimental setup, dc/dc boost converters, and the measurement/control board

In experimental studies, semiconductor switches' duty cycle D ratios were changed from 0.1 to 0.9 to show the effect of normalized input current ripple change of the dc/dc boost circuits. The output voltage of SBC and ISBC circuits is set to a constant 200 V. Measurements in the circuits were recorded at different duty cycle D rates. Fig. 9 (a) shows the voltage and current waveforms of the SBC circuit when the duty cycle D is 0.3. In this case, the input voltage of the SBC circuit is 142.7 V, and the current is 8.749 A. The inductor current ripple value is Δi_{L_SBC} 1920 mA.

The output current of the SBC circuit is 5.821 A, the output ripple voltage Δv_{out_SBC} is 60 mV, and the current Δi_{out_SBC} is 0.80 mA. Fig. 9 (b) shows the experimental results of the duty cycle D ratio of 0.5. In this case, the circuit's inductor voltage and current ripple are Δv_{out_SBC} 110 mV and Δi_{out_SBC} 1.1 mA, respectively. Gate signals of SIC MOSFETs were given on oscilloscope screens.



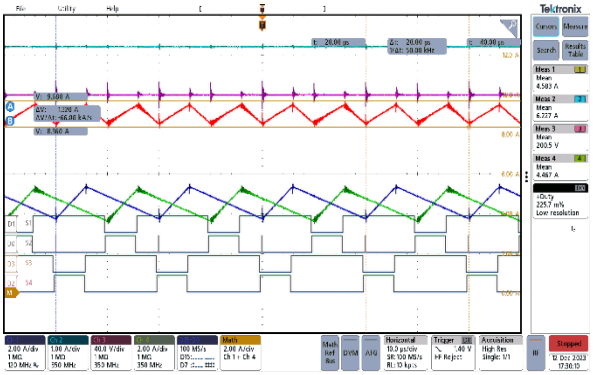
(a)



(b)

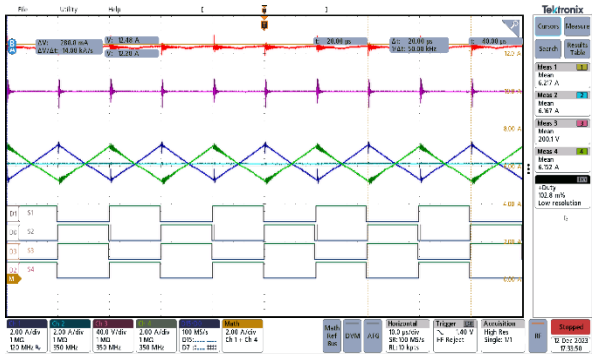
Figure 9. The input/output parameters' waveforms of the dc/dc synchronous boost converter circuit, (a) *D* is 0.3, (b) *D* is 0.5, (Ch1:v_{bat}, Ch2: i_{bat}, Ch3: v_{out}, Ch4: i_{L_SBC})

Experimental results of the ISBC circuit at different duty cycle rates under the same operating conditions have been conducted. The oscilloscope results are given in Fig. 10. In the operating state of duty cycle D 0.3, shown in Fig. 10 (a), the voltage and current waveforms of the ISBC are 141.4 V and 2.1 A, respectively. In this case, the inductor current value on the first layer of the circuit is 4.583 A, and the inductor current is ripple ΔiL_ISBC 1.9 mA. The duty cycle D ratio of the ISBC circuit shown in Fig. 10 (b) is 0.5. In this case, the input voltage and current are 102 V and 2.93 A, respectively. The inductor current at the first layer of the ISBC circuit is 6.217 A, and the inductor ripple current is ΔiL_ISBC 2.21 mA.



(a)

Figure 10. The input/output parameters' waveforms of the dc/dc interleaved synchronous boost converter circuit, (a) *D* is 0.3, (b) *D* is 0.5, (Ch1: i_{L_2}, Ch2: i_{bat}, Ch3: v_{out}, Ch4: i_{L_1}, Math: i_{L_ISBC})



(b)

Figure 10.(cont.) The input/output parameters' waveforms of the dc/dc interleaved synchronous boost converter circuit, (a) *D* is 0.3, (b) *D* is 0.5, (Ch1: i_{L_2}, Ch2: i_{bat}, Ch3: v_{out}, Ch4: i_{L_1}, Math: i_{L_ISBC})

Fig. 11 shows the experimental measurement and analytical normalized input current ripple graph of the ISBC circuit depending on duty cycle change. Since the duty cycle *D* ratio cannot be 0 and 1 in the experimental studies, experiments were carried out with the duty cycle *D* ratio being a minimum of 0.1 and a maximum of 0.9. As the duty cycle *D* ratio approaches 0.5, the normalized input current ripple $\Delta i_L/\Delta i_{bat}$ value becomes 0.13 in the ISBC circuit.

Fig. 12 shows the experimental measurement and analytical normalized output capacitor current graph of the SBC and ISBC circuit depending on duty cycle change. In the experimental results, at the duty cycle ratio of 0.5, the normalized output capacitor current is 0.5 and 0.12 for the SBC and ISBC circuits, respectively.

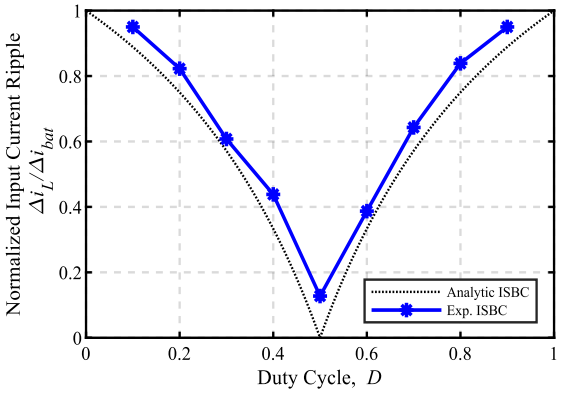


Figure 11. Experimental measurement and analytical normalized input current ripple graph of the ISBC circuit depending on duty cycle change

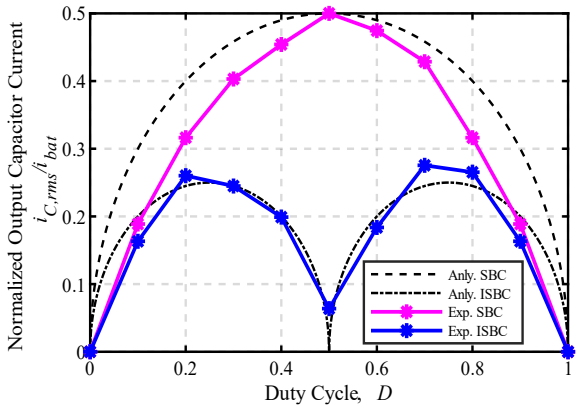


Figure 12. Experimental measurement and analytical normalized output capacitor current graph of the SBC and ISBC circuit depending on duty cycle change

When the results are analyzed, it is observed that the inductor current value in the ISBC circuit is shared equally with that of the SBC circuit. It is seen that the ISBC circuit works more efficiently than the SBC circuit under the same conditions.

The ripple current on the capacitor induces power losses across its equivalent series resistance, leading to heat-related issues and a potential reduction in the capacitor's lifecycle. Therefore, reducing ripple current helps mitigate the negative impact of temperature on the capacitor's lifecycle. The SIC MOSFET has drain-source on-state resistance, and the diode has the forward voltage. An increased current ripple value will lead to a rise in the maximum current value, consequently causing power losses on semiconductor components due to the drain-source on-state resistance and the forward voltage.

It has been observed that the current value on the inductor decreases thanks to the interleaved structure of the ISBC circuit. In addition, under the same operating conditions, inductor ripple current, output voltage, and current ripple values decreased compared to the SBC circuit. This ensures that the passive circuit elements are reduced in volume and mass. In addition, since the current passing through the inductor decreases, it reduces circuit losses. It shows that ISBC circuit topology should be preferred in high-power EV charging applications.

4. CONCLUSION

This study shares the performance results of the dc/dc boost converter topologies used in electric vehicles at different duty cycles. Battery charge/discharge circuits in the EVs must be low volume and high efficiency. This study gives experimental results of the synchronous boost and interleaved synchronous boost converter topologies in the literature. Experimental test results prove that the ISBC circuit is the most efficient topology. It has been observed that the ISBC circuit topology operates at 1249 W output power, 0.91 A output current ripple, and 99.09% efficiency. These results show that using ISBC circuit topology in high-power charge/discharge applications for EVs is advantageous.

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DECLARATION OF ETHICAL STANDARDS

This article's author(s) declare that the materials and methods used in this study do not require ethical committee permission and/or legal-special permission.

AUTHORS' CONTRIBUTIONS

Hakan Akca: Contributed to the experimental studies, paper layout, creation of sections, and paper writing process.

Ahmet Aktas: Contributed to the experimental studies, paper layout, creation of sections, and paper writing process.

CONFLICT OF INTEREST

There is no conflict of interest in this study.

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